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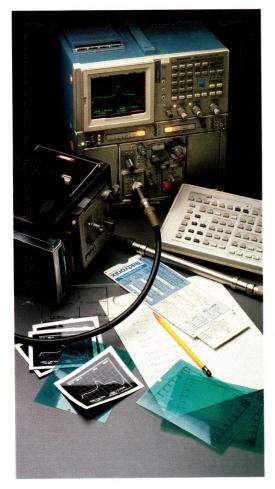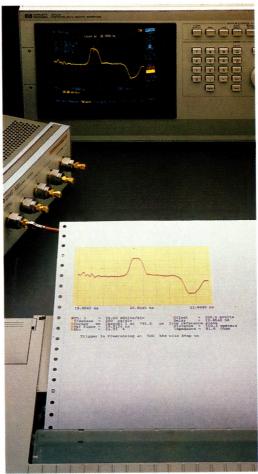
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

SILICON PRESSURE SENSOR (16UM THICK) ON GLASS 20 MIL THICK, DT=100C

Pressure-sensor design simplified by CAD/CAE

There are two sides to this story...

The Bettman Archive Inc.

Making something very small can be truly revolutionary.

At first people scoffed. Some laughed out loud. But the people's car set a new size standard for an entire industry.

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solve, ensures that reliability is designed in, built in, and tested. So we can solve big problems. With small, but revolutionary, innovations.

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Neonatal sensor for SensorMedics oximeter measures pulse and blood gases.

On the cover: *Pressure sensors and transducers are achieving high marks for performance, thanks in part to device manufacturers using CAD/CAE techniques. See pg 106. (Photo courtesy Nova Sensors)*

∇BPA ABP Φ

Third-party graphics-software packages for IBM PCs and compatible computers can ease your software-writing chores (pg 55).

TECHNOLOGY UPDATE

Attention-grabbing, colorful graphics can dramatically enhance the software you write, regardless of whether you're developing it for your company's internal use or for customers.—*Margery S Conner, Regional Editor*

Monolithic phase-locked-loop (PLL) circuits provide an elegant way to achieve frequency demodulation or digital selection of frequency. —*Tarlton Fleming, Associate Editor*

PRODUCT UPDATE

DESIGN IDEAS

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

Express Request

128 TIMES THE MEMORY DEPTH AND LIGHT-YEARS AHEAD OF THE COMPETITION.

Only the Tek DAS9200 with its new 92A90D acquisition module gives you a memory depth of 128K bits-per-channel— 128 times the depth provided by the most popular alternatives. No wonder it alone lets you see so much, so easily, for so many complex applications.

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EDITORIAL   49

Establishing a tariff that funds US R&D efforts might be a suitable alternative to mandating artificially high semiconductor prices.

NEW PRODUCTS

PROFESSIONAL ISSUES   255

Milt Scovill's long and winding road.—*Deborah Asbrand, Associate Editor*

LOOKING AHEAD   267

Surveys quiz CASE users and vendors. . . PC-board ATE market to reach $1.1B by '93.

DEPARTMENTS

Odds are 50-50 your perfect ASIC is a perfect dud the first time you plug it in.

That's why Mentor Graphics lets you combine ASIC and board circuitry in a single simulation.

Trouble in ASIC paradise.

The big day has arrived.

Your first gate array is back from the foundry. With high expectations, you plug it into your board and power up.

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Library support is an ideal benchmark to gauge the true worth of an electronic design automation system. The more diverse and plenti-ful the component modeling libraries, the greater the design capability. It's as simple as that.

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How the fa

Our new 7.5ns PAL® device is fast enough to prove that standard logic shouldn't set the standard anymore.

It's also fast enough to finally let today's new microprocessors run at the speeds for which they were designed—breathtaking.

Raising your standard.

How fast would you like your standard logic?

How about faster than any TTL logic around? Even FAST™ or AS? You've got it with the 7.5ns PAL device.

And the fact that you can config-

7.5ns PAL Device vs. FAST & AS				
SSI/MSI		FAST	AS	7.5ns PAL Device
Combinatorial				
74138	tPD	8.0	10.0	7.5
Decoder				
74151	tPD	11.0	15.0	7.5
Mux				
Register/Latch				
74374	tCO	10.0	9.0	6.5
Octal Register				
74373	tPD	8.0.	6.0	7.5
Octal Latch	tLEO	13.0	11.5	7.5
Counters				
74161	tS	5.5	8.0	7.0
Four bit Ctr	tCO	11.0	13.5	6.5
74269/869	tS	2.5	5.0	7.0
Eight bit Ctr	tCO	10.0	11.0	6.5

ure it yourself means you can get exactly what you want.

If you want to redesign something, you change the PAL device. Not the board.

Not only is this the fastest way to get high speed logic, it's also the most practical. One 7.5ns PAL device replaces two to six standard TTL devices.

Which cuts down on board size.

And cuts down chances for a device failure.

st get faster.

What to give the microprocessor that has everything.

We suggest the first PAL device that can keep up with it.

The 7.5ns PAL device runs at 74 Mhz. It can deliver the speed the new high performance microprocessors need.

Processors like the 29K, the 386 and the 68030.

This PAL device delivers 25% more speed than any other PAL device.

We even have the fastest 22V10.

Our 15ns 22V10 runs at 50Mhz. That's 10ns faster than anyone else on the market. And it lets you run at twice the rate of the new 25Mhz microprocessors.

We've been shipping 20 pin 10ns

PAL devices for eighteen months. And now you can get the new 24 pin 10ns PAL device as well.

There's plenty of service and support to get and keep your project moving. And all our fast PAL devices are available in volume when you need them. Now, for example.
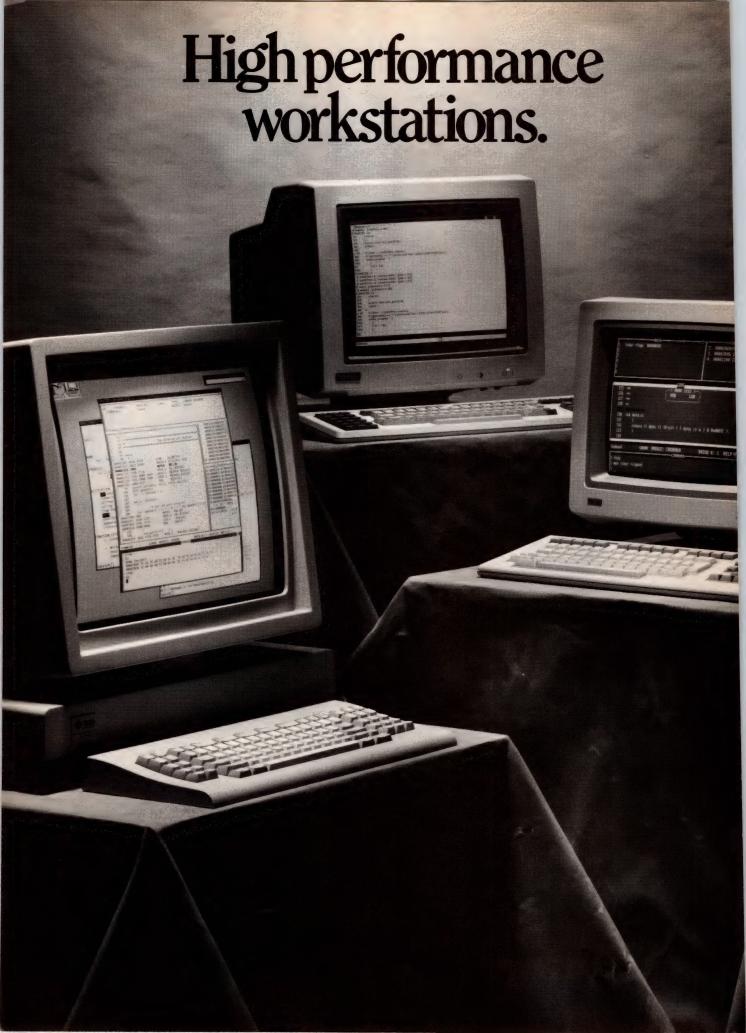
For all the facts about our fast PAL devices, drop us a line.

Because you can never be too fast.

Advanced Micro Devices ◿
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For more information write "7.5ns PAL device" on your letterhead and send to:
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"Listen, the future of this product line is riding on my next design automation decision. Not to mention my job."

"I hear you. So tell me more and let's figure out how HP can help you make some of those decisions."

"Well, first, we're feeling enormous pressure to get products out faster. The key is designs that'll go through manufacturing the first time. If we're going to stay competitive, we've got to tackle the overall product development process—and it starts right here in design."

Look, HP's gone through the same thing. Our own divisions deal with the same problem daily. We came up with a solution called DesignCenter. It combines our electronic design automation tools with the rest of the process to produce a high degree of manufacturability right from the start—in design."

"That's exactly what we need. A single data path from design right on through production and out the door. If we could somehow combine electronic design with microprocessor development and mechanical engineering and tie it into manufacturing and test, we'd be a lot happier. Are you saying HP can do that for us now?"

"We're not there 100% yet. Nobody is. But that's the whole idea behind our DesignCenter. Right now, we've got the broadest set of EDA tools there is. Match them up with the HP test and measurement tools you've used for years, and you'll be way ahead of the game."

"We've always counted on HP test equipment. But how does that relate to your EDA tools?"

"We were able to bridge the gap between design and prototype test. Now you can create higher quality tests—faster, too—by transferring data directly between our logic analyzers and simulation. And the design and layout tie directly into HP board test systems."

"That's terrific. But testing is only one part of the process. We're making decisions on everything from ASICs and PLDs to microwave hybrids to multi-layer PCBs. And they all have different parts and technologies. I'll tell you, it's impossible to keep up."

"We agree, it's a big problem. But that's the reason we have digital, analog, and microwave CAE tools for design, simulation, and layout. We even support it all with information management to handle the tough tradeoffs your team has to make in choosing between all the technologies and complex interactions."

"There's one thing that's always a concern. We've got systems in here from some of your competitors. If we go with HP, can you fit into our existing environment?"

"Absolutely. Using either off-the-shelf or customized interfaces, we'll help you integrate HP tools into your existing systems. And, since HP supports EDIF and IGES standards, you'll have the flexibility you need down the road."

"Speaking of standards, tell me about your platforms."

"Well, HP is among the industry leaders in standardization because the marketplace is demanding it. Our family of workstations and servers supports UNIX and networking standards. They thrive in a multi-vendor environment, making it easier to get your job done right the first time. That's the bottom line these days."

"I get the feeling you understand that we're interested in a lot more than just tools. I mean, you seem to be talking about more than hardware and software."

"I am. HP is totally committed to this idea of getting more correct-by-design products through your plant. We are talking about a lot more than the tools. We'll sit down with you and help create a system that meets your needs...not ours or somebody else's. And I mean we'll get right down to solving problems and training your people. That's what we do better than anyone else."

"I want to keep talking about this whole thing. And I want to include some other engineers, too. What are you doing next Wednesday?"

"I've got a feeling I'll be back here."

"Right."
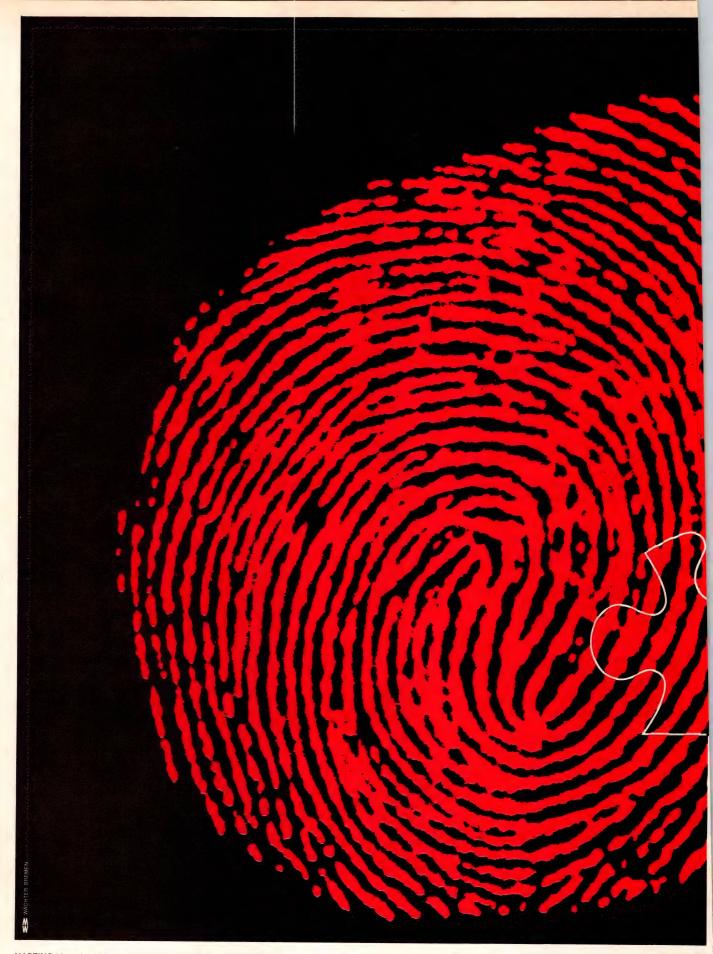
"Name a time."

The dialogue continues...

More and more project managers are talking to HP about EDA tools and DesignCenter. Start a dialogue today. Call toll free. Ask for information on HP Electronic Design Automation and bridging the gap from design to prototype test: 1-800-752-0900, **Ext.** C215.

we never stop asking What if...

HEWLETT PACKARD

SOME THINGS CAN'T BE COPIED.

That's something we at HARTING learned long ago. For instance, our engineers and designers invested years of hard work to develop our "HARTING Industrial HAN® Connector". Their goal was to get every little detail just perfect so that state-of-the-art production processes and high-tech robots could be used to produce the definitive connector.

Well, our HAN® Connectors were a big success worldwide – and they still are. Of course, it didn't take long before similar connectors with similar names hit the market. But the original HAN® still hasn't been equalled. Because it's unique – just like your fingerprints. After all, it's the only one produced in completely automated high-tech production facilities. Each individual component part is made of the very best material available. And each part has to go through a whole series of quality-control stations. That's how we manage to make sure that every HAN® Industrial Connector that leaves our plant is absolutely perfect. And the millions of our connectors in use throughout the world today are proof of this unprecedented reliability.
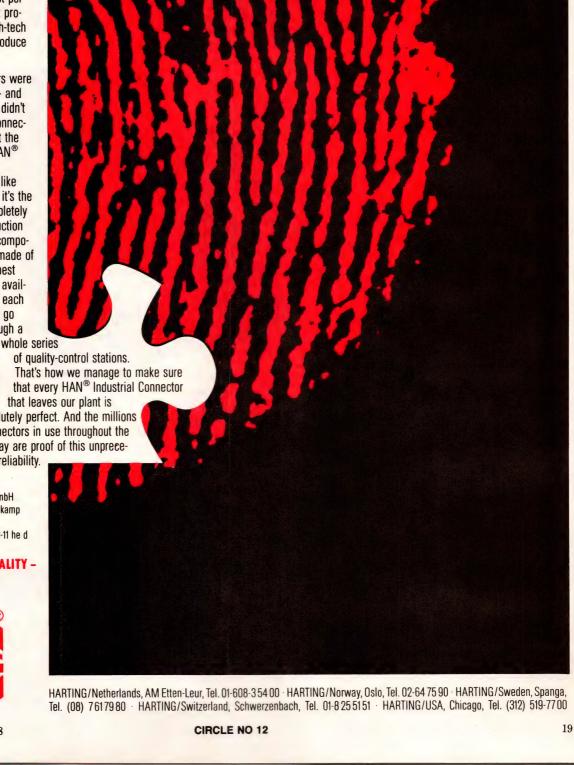
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NEWS BREAKS

EDITED BY JOANNE CLAY

8-BIT HALF-FLASH ADC INCLUDES TRUE SAMPLE/HOLD AMPLIFIER

The LTC1099 from Linear Technology Corp (Milpitas, CA, (800) 637-5545) is a half-flash 8-bit A/D converter that converts in 2.5 μsec typ. A true sample/hold amplifier is included on the chip; it allows the ADC to convert 5V p-p signals at as much as 167 kHz, or signals with slew rates as high as 20V/μsec. The LTC1099 is pin compatible with the AD7820 and the ADC0820; these older devices can complete the A/D conversion in 1.5 μsec, but have pseudo-S/H amplifiers that can accept signals with a maximum slew rate of 0.1V/μsec or a bandwidth limit of 7 kHz. (To acquire signals with higher frequencies, these older devices require an external S/H amplifier, which is usually expensive.) The LTC1099 costs $8 (100).—David Shear

EVALUATION MODULE PROVIDES INTERFACE TO CONSUMER ELECTRONIC BUS

The SEM-200 Smarthome evaluation module from CyberLynx (Boulder, CO, (303) 444-7733) provides easy access to the Consumer Electronic Bus (CEBus) currently being developed as a standard under the sponsorship of the EIA. The CEBus is a low-cost, multimedia LAN designed to interconnect appliances, audiovisual equipment, and other household devices. The $450 SEM-200 acts as a network node and LAN analyzer that monitors network traffic. You can connect a PC or a dumb terminal to the unit's RS-232C interface to observe activity on the CEBus network. The module provides digital inputs and relay outputs that allow you to add CEBus capability to a wide range of product prototypes. CyberLynx and Texas Instruments (Dallas, TX) are jointly developing a line of interface ICs for the CEBus.—Steven H Leibson

PC/AT GPIB INTERFACE OFFERS 1-MHz DMA TRANSFERS

If you have an IBM PC/AT or compatible computer, you can use the AT-GPIB expansion card from National Instruments (Austin, TX, (515) 250-9119) to speed your IEEE-488 communications. This $495 interface lets your 80386- or 80286-based computer communicate with as many as 13 instruments at data-transfer speeds reaching 1M byte/sec. Bidirectional FIFO buffers let the device read at 1M byte/sec, write at 700k bytes/sec, and execute GPIB commands at 320k bytes/sec. The AT-GPIB comes with the NI-488 software package, which includes BASICA, Quick BASIC, and a binary MS-DOS device driver with more than 30 IEEE-488 functions. The board can use one of 11 selectable lines to interrupt the host PC.—J D Mosley

ANALOG MEASUREMENT MODULE OFFERS 50-kHz THROUGHPUT

For applications requiring 16-bit A/D conversions, you can select the AMM2 Master Analog Measurement Module from Keithley Instruments (Cleveland, OH, (216) 248-0400) for 50-kHz data transfer. The $1155 module offers 16 single-ended or eight differential analog inputs, a crystal-controlled oscillator for jitter-free FFT analysis, and an external trigger. The AMM2 provides programmable operating parameters that let you control gain and configure inputs. The unit automatically performs internal calibration when used with the manufacturer's Soft500 and Quick500 data-acquisition software.—J D Mosley

MICROCOM NETWORKING PROTOCOL INCLUDED ON MODEM CHIP SET

Sierra Semiconductor (San Jose, CA, (408) 263-9300) is changing the program of its SC11011 modem processor: The new version, the SC11013, will implement the Microcom Networking Protocol (MNP). This protocol has been used for many years to provide error-free communications in the banking industry. The MNP is a data-

communications protocol for full-duplex, error-free communication over ordinary voice-grade telephone lines. Software-communication packages use similar techniques, but these tend to be machine dependent. MNP exists in firmware within the modem, so any computer or terminal can be used. The protocol includes a data-compression algorithm that provides an effective data rate as high as 2900 bps with a 2400-bps modem. The SC11013 modem processor and the SC11006 modem analog peripheral together cost $33.50 (25,000). You'll also need some extra components such as a RAM, a USART, and some logic circuits; you can obtain all the necessary parts for $7.50. In effect, you'll be able to build a modem that implements the MNP for less than $11 over the cost of producing a standard 2400-bps modem.—David Shear

GRAPHICS CHIP AND MATH COPROCESSOR INCREASE DRAWING SPEED

The TMS34020—the latest version of the TMS34010 graphics processor from Texas Instruments (Dallas, TX, (800) 232-3200 ext 700)—can make use of the company's new TMS34082 floating-point coprocessor to accelerate graphics functions such as coordinate transformations. In addition, the 34020 has 25% more microcoded graphics primitives, so it can render the primitives faster than can software-based primitives. All 34010 object code is upwardly compatible with the 34020. The 34010 has a 32-bit internal and a 16-bit external data bus; the 34020 has an internal and an external 32-bit data bus. The 34020 runs at from three to 20 times the speed of the 34010. Samples of both the 34020 graphics processor and the 34082 math coprocessor will be available in the fourth quarter of 1988 at $500 each; production quantities will be available in the first quarter of 1989. You can expect to see the price of the 34020 drop by an order of magnitude within the next 18 months.—Margery S Conner
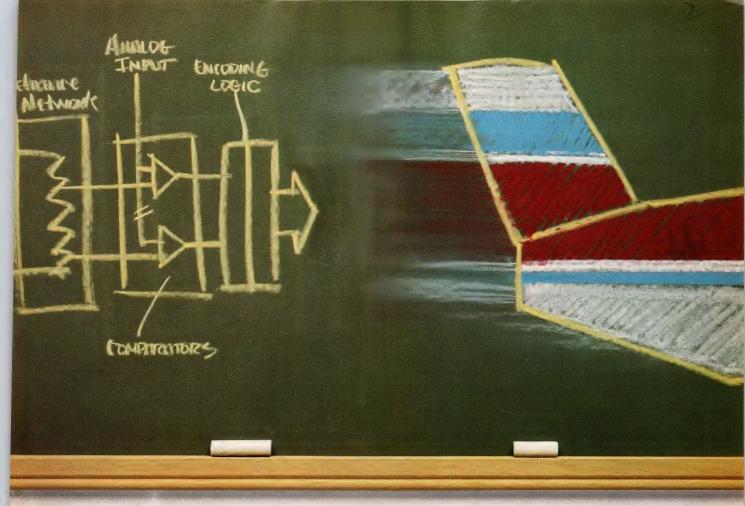
INTERFACE UNIT CONVERTS SCSI TO ETHERNET

The Nodem allows you to connect your personal computer to Ethernet via your computer's SCSI port. The unit is completely external; it doesn't use your computer's expansion slots, and it has its own wall-mounted power supply. You adapt the unit to your system configuration by using software supplied with the unit. The Nodem works with IBM PCs and compatibles, the IBM PS/2, and the Apple Macintosh. It's transparent to AppleTalk.

The units are made by Adaptek (Milpitas, CA, (408) 945-8600), but will be marketed primarily by LAN-system suppliers and value-added resellers. The standard Ethernet version will cost approximately $545; the Cheapernet and twisted-pair versions will sell for about $595. The units will be available with software for Macintosh systems in September; software for IBM systems will be available in early 1989.—Richard A Quinnell

MULTITASKING, RESIDENT BASIC COMPILERS TARGET EMBEDDED SYSTEMS

The MTBasic compilers from Softaid Inc (Columbia, MD, (301) 964-8455) provide multitasking Basic and a kernel operating system for diskless, embedded-processor systems employing the Zilog Z80 or Z280, the Hitachi 64180, or the Intel 8088 μPs. The compilers reside in a ROM on the target system and offer a conventional programming environment similar to that provided by compilers running on personal computers. The vendor supplies source code for each compiler, allowing you to tailor features of the language for your specific application. Each compiler costs $6500.—Steven H Leibson

NEWS BREAKS: INTERNATIONAL

ADA COMPILERS MAKE TRANSPUTERS SUITABLE FOR MILITARY SYSTEMS

If you're using Inmos Transputers in embedded systems for military contracts, you'll probably be required to write the system software in the Ada programming language. Two compilers being developed by Alsys SA (La Celle Saint-Cloud, France, TLX 697569; in the US: Waltham, MA, (617) 890-0030) can help. The compilers generate code for any of the Inmos 16- and 32-bit integer Transputers or the IMS-T800 floating-point Transputer. One is a cross-compiler that runs on DEC VAX computers under VMS; the other is a host compiler that runs under MS-DOS on IBM PCs and compatibles to which you've added a T800-based add-in card. For a medium-sized VAX, the cross-compiler is expected to sell for around Fr 250,000. The PC-based host compiler will probably cost around Fr 50,000.

Although these compilers won't be available until the middle of 1989, you can start software development now by using one of the company's currently available VAX-based validated Ada compilers. Because all the company's Ada compilers share a common-root front-end and intermediate code, the software you write with one of the available compilers will recompile to Transputer code when run through the Transputer's Ada compiler. To meet military-hardware requirements, Inmos (Bristol, UK, TLX 444723; in the US: Colorado Springs, CO, (719) 630-4000) plans to introduce a version of the T800 Transputer that's qualified to MIL-STD-883C during the first quarter of 1989. The company will follow that product with military versions of the 16- and 32-bit integer Transputers later the same year.—Peter Harold

SIEMENS AND AMD AGREE TO DEVELOP PIN-COMPATIBLE ISDN CHIP SET

Siemens Components (Munich, Germany, TLX 521000; in US: Santa Clara, CA, (408) 980-4500) and Advanced Micro Devices (Sunnyvale, CA, (408) 732-2400) have agreed to jointly develop and supply ICs for the telecommunications and data-communications industry, with emphasis on an ISDN chip set. You will be able to obtain pin-compatible devices from both companies, selecting from a set of 15 devices (13 Siemens chips and two AMD chips) that are based on a common architecture. PSB2110 ISDN terminal adapter circuit, PEB2085 ISDN subscriber-access controller, and the Am79C401 integrated data-protocol controller. The companies will begin by offering each other's parts; then they'll exchange manufacturing technology to build a true alternate-source capability for the entire set of devices.—Richard A Quinnell

TOSHIBA FORMS TUNNEL JUNCTION FROM SUPERCONDUCTOR MATERIAL
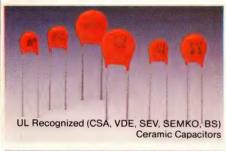
According to reports in the Japanese press, Toshiba Corp has created a thin-film technology for high-temperature superconducting material that may make commercial superconducting computer chips possible. The company has successfully combined lead and yttrium-based superconductor material, forming a tunnel junction. The firm used this procedure to make a prototype, and confirmed that the device's voltage could be used in on/off switching functions. These results reportedly represent the first time anyone has confirmed such a function in a superconducting device.—Joanne Clay

You wouldn't do this with your Analog VLSI devices.

You'll have to if you go to most ATE companies for a solution to today's sophisticated "system silicon" testing problems. Because all you'll get is a make-shift tester. And that means resigning yourself to man-months of custom hardware work integrating analog and digital instrumentation. And putting up with the long hours of low-level software development that go with custom solutions. Worse, you can expect these delays to cut your chances of getting your product to market on time.

Teradyne now has a simple answer to this complex testing problem. The A500 Analog VLSI Test System. It's the first of a new generation of systems specifically for AVLSI "system silicon" devices. A test system that can help you cut critical product development time by months or even years.
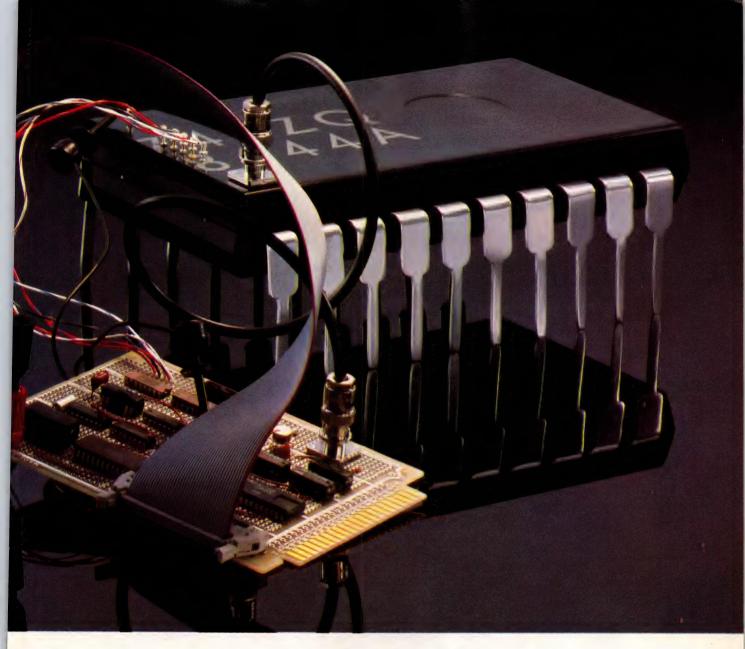
One Test System, Once and for All
With AVLSI devices you won't get fast design feed-back, unless you test individual components—the "building blocks" of system silicon. And you won't comply with customer and industry requirements if you don't do complete "system" functional testing. With conventional test systems it means two of every-thing. Two testers, two test programs, two insertions, two data bases. And more than twice the time to get to market.

The A500 allows you to do it all with one system. So there's only one system to program. One insertion to make for both component and functional testing. And only one data base to work with. Which means significantly less time to market.

Vector Bus II™: the Great Integrator
The heart of the A500 is Teradyne's unique Vector Bus II architecture. It integrates analog and digital VLSI test capability at the system level. Which means you won't have to build special applications hardware for every new device you design. Vector Bus II eliminates that costly custom-work bottleneck

Why accept it in an Analog VLSI Test System?

with such features as TimeMaster™ Synchronization, Mixed-Signal Event Control, and MultiSource Data Mixing.

A Picture's Worth a Thousand Keystrokes

The A500 also revolutionizes program development. Our IMAGE™ (Interactive Menu-Assisted Graphics Environment) software gives you graphics programming as powerful as device designers' CAD/CAE tools. Using a mouse to control multiple windows, pop-up menus and software "power tools," you move ideas rapidly from mind to screen. And much faster to market.

Teradyne's new A500 is the only test system with the features you need to win the race for Analog VLSI market opportunities. To find out more, call Beth Sulak at (617) 482-2700, ext. 2746. Or call your nearest Teradyne sales office or write: Teradyne, Inc., 321 Harrison Avenue, Boston, MA 02118.

TERADYNE

We measure quality.

SIGNALS & NOISE

EE seeks source of basic, general-purpose algorithms

The company I work for designs medical test equipment, and most of our work involves 8-bit microprocessors in embedded-control applications. We use IBM PCs and compatibles as development tools, and there is plenty of software for that environment. However, there is no source that I can find for writing the fundamental algorithms that we take for granted in a high-level language. What I'm very anxious to find are sources for algorithms in general terms that can solve the problems we often encounter.

For instance, floating-point routines, sine, cosine, tangent, square root, graphics, and ASCII-to-binary routines are becoming much more important to our needs. Where can the fundamental algorithms be found to implement these functions?

The ideal solution for me would be a reference book (or books) that described at a flowchart level how to code these algorithms independently of a specific processor. This method allows the designer to pick the best hardware solution without depending on the availability of some special-purpose software that is written for only one µP.

In the accompanying **table,** I've listed some of the particular needs that I've run across; it's a wish list of mysteries I'd love to see revealed.

If you could suggest some places to look or publications that answer some of these questions, I'd appreciate it very much. I think this need is shared by a great many engineers. Perhaps someday your magazine could publish the solutions to these algorithms in generic format.

Alan Clark
Dynatech Nevada
Carson City, NV

(*Ed Note: We'd like to enlist the readers' help on this one. If you know of any sources for the algo-*

FUNCTION	DESCRIPTION
FLOATING POINT	ADD, SUBTRACT, MULTIPLY, DIVIDE
TRIGONOMETRY	SINE, COSINE, TANGENT
SQUARE ROOT	INTEGER AND FLOATING-POINT SOLUTIONS
INTEGER TO FLOATING	CONVERSION
FLOATING TO INTEGER	CONVERSION
GRAPHICS	HOW TO MODEL A BIT-MAPPED PLANE; ROUTINES FOR DRAWING A LINE BETWEEN TWO POINTS; CIRCLES AND OTHER SHAPES
ASCII TO INTEGER	CONVERT ASCII STRING TO SIGNED/UNSIGNED INTEGER
INTEGER TO ASCII	CONVERT INTEGER TO SIGNED/UNSIGNED ASCII STRING

SIGNALS & NOISE

Fault-critical applications need bugless processors

Steven H Leibson's article "Fault-tolerant design spans terrestrial and space applications" (EDN, April 28, 1988, pg 180)—while naturally, in the space available, is able to offer only superficial treatment of this important subject—is particularly timely with regard to Intel's announcement of its 80376 microprocessor for embedded applications.
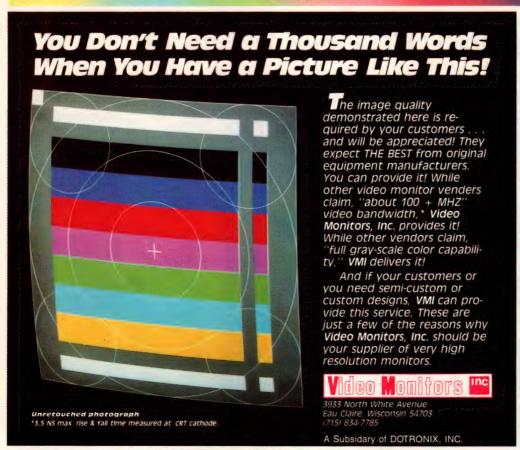
Embedded processors, especially high-end 32-bit machines, are primarily intended for fault-critical applications such as those outlined in Steve's article. To use a processor in a fault-critical application, one must have a high level of confidence in that processor's integrity—its freedom from undocumented faults that can lead to abnormal behavior. The 80386, upon which the 80376 is based, however, is becoming notorious for its number of errors, and Intel's *Stepping Information* (essentially a bug list showing possible ways to work around those bugs) is now at Revision D, and possibly even at Revision E. Is this an architecture one can have confidence in for a critical application?

That question leads me to a crucial point that Steve doesn't mention in his article: the problems of common-mode faults and the question of software in redundant systems.

The inexperienced may be tempted to think that redundancy is a potential panacea, but that's not so. Suppose that you construct a dual-redundant system, using the same processor and the same software in each channel. If that processor contains a fault that causes the system to crash for some combination of data and instructions, both channels will fail simultaneously.
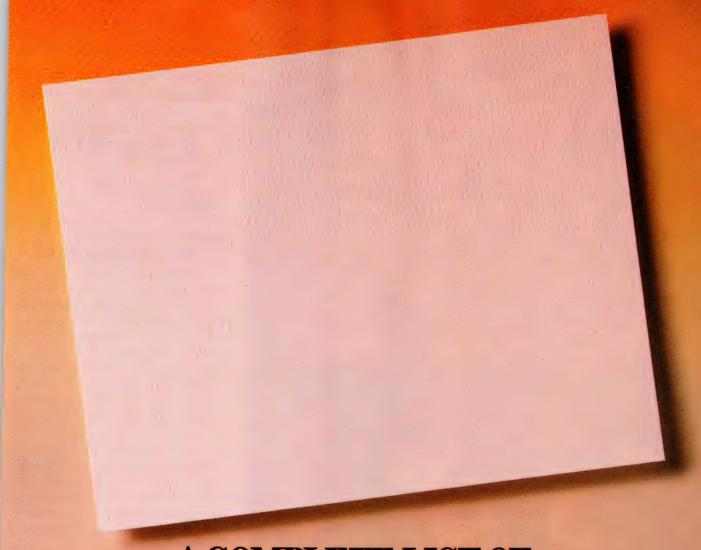
What is needed is a processor that has been proven to contain no bugs, and that behaves in a predictable manner for such cases as illegal op codes. Such a processor would not, of course, protect against erroneous (but legal) software operations, but it would remove at least one level of uncertainty from the design of fault-critical systems. Such a processor is already commercially available: It has a RISC architecture, 32-bit data, predictable behavior, and an architecture that has been mathematically verified to be correct. I refer, of course, to the MAS-1908 Viper, which is available from Marconi and supported by Assurance Systems. Unfortunately, in the US this device seems to suffer from the NIH ("not invented here") syn-

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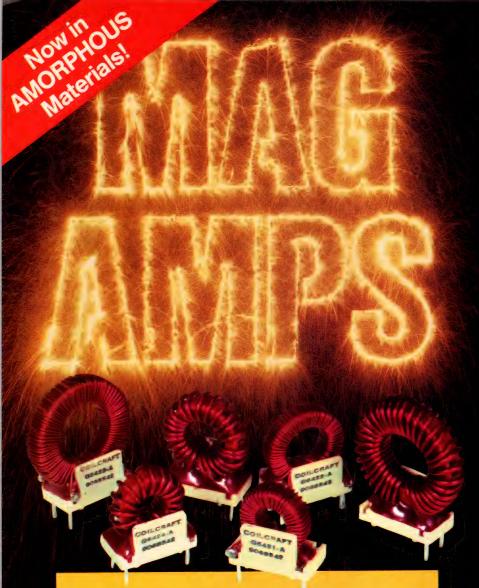
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SIGNALS & NOISE

drome, so I and others will have to continue to ensure our safe descent into Logan Airport at night, in a thunderstorm, by the unproven (but not disproven) power of prayer.
Cris Whetton
President
Assurance Systems
Levittown, PA

Resistor would solve discharge-current problem

The Schmitt-trigger switch-debounce circuit appearing in the Design Idea "Switch debouncer uses few parts" (EDN, February 18, 1988, pg 244) will ultimately be unreliable, because excessive discharge current from the 4.7-μF capacitor will damage the switch contacts (S1). This problem would be even more troublesome should the designer choose a switch designed for low-current switching (an appropriate choice for the type of circuit shown). A 220Ω resistor in series with the switch would solve the problem and leave the circuit's performance essentially unaffected.
Rod Deakin
Director of Engineering Services
Arix Corp
San Jose, CA

(*Ed Note: In fact, the circuit contains a number of problems. The author is submitting a corrected version of the Design Idea; it'll appear in a future issue of EDN.*)

Omission

Part 5 of the Decade 90 Series (EDN, April 28, 1988, pg 180) neglected to mention the location of Fail-Safe Technology Corp, a consulting firm specializing in reliable-system design. The company is based in Los Angeles, CA.

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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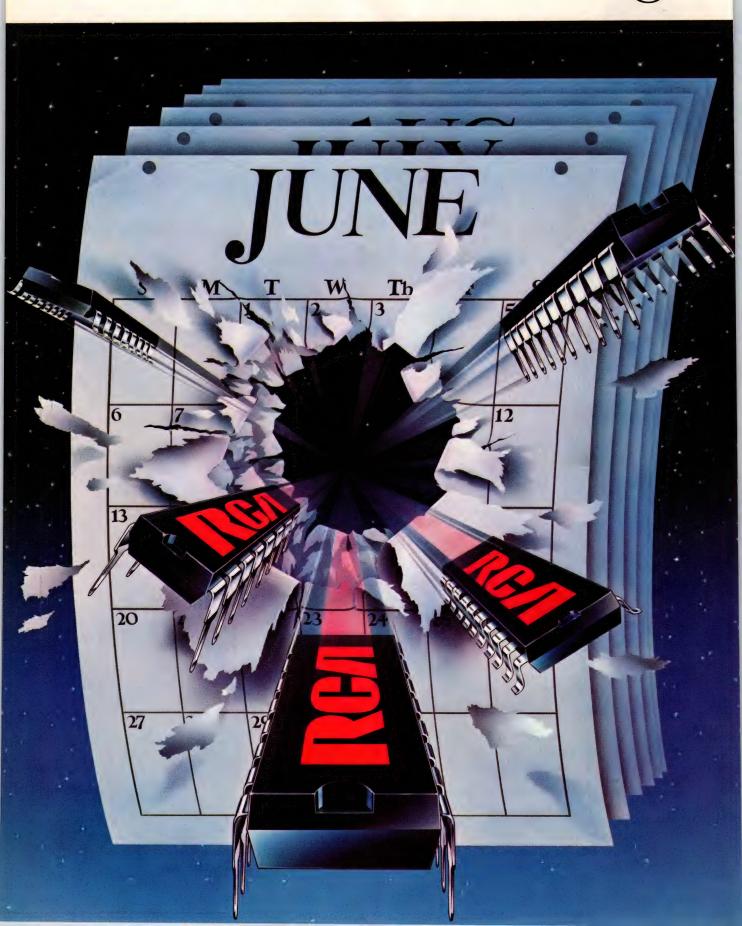
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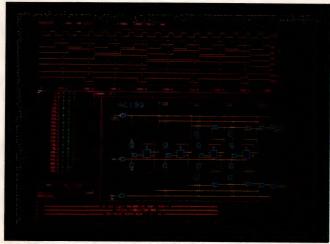
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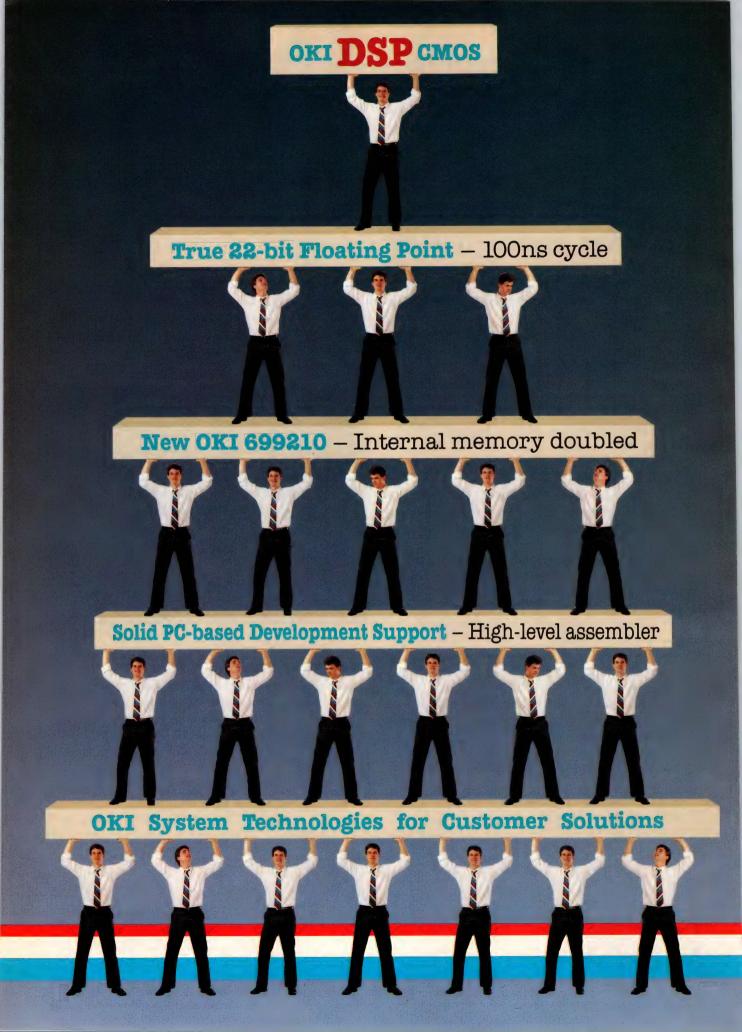
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International Conference on Handheld Computing, Corvallis, OR. Eric Gakstatter, ICHC, 301 NE Byron Pl, Corvallis, OR 97330. (503) 752-5456. August 4 to 6.

CASE Benchmarks: A Product Comparison Seminar, Atlanta, GA. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (617) 470-3870. August 10 to 12.

Microwave Circuit Design I: Linear Circuits (short course), College Park, MD. University of Maryland Center for Professional Development, University Blvd at Adelphi Rd, College Park, MD. (301) 985-7195. August 15 to 19.

Microwave Circuit Design II: Nonlinear Circuits (short course), College Park, MD. University of Maryland Center for Professional Development, University Blvd at Adelphi Rd, College Park, MD. (301) 985-7195. August 22 to 26.

Midcon, Dallas, TX. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (800) 421-6816; in CA, (213) 772-2965. August 30 to September 1.

Surface Mount '88, Marlborough, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. August 30 to September 1.

Modern Electronic Packaging (seminar), Santa Clara, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. September 7 to 9.

International Test Conference, Washington, DC. Doris Thomas, ITC, Box 264, Mount Freedom, NJ 07970. (201) 267-7120. September 12 to 14.

Worst-Case Circuit Analysis (seminar), Boston, MA. Design and Evaluation, 1000 White Horse Rd, Suite

CALENDAR

304, Voorhees, NJ 08043. (609) 770-0800. September 12 to 14.

C Programming Workshop (short course), Seattle, WA. SSC, Box 55549, Seattle, WA 98155. (206) 527-3385. September 12 to 15.

12th International Fiber Optic Communications and Local Area Networks Exposition, Atlanta, GA. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (800) 323-1088; in MA, (617) 232-3111. September 12 to 16.

Connector and Interconnection Technology Symposium, Dallas, TX. Electronic Connector Study Group, 104 Wilmot Rd, Suite 201, Deerfield, IL 60015. (312) 940-8800. October 3 to 5.

IEEE International Conference on Computer Design: VLSI in Computers and Processors, Port Chester, NY. Gail Clanton, IEEE, 1730 Massachusetts Ave NW, Washington, DC 20036. (202) 371-1013. October 3 to 5.

Autotestcon, Minneapolis, MN. Steve Palmer, Unisys, 3333 Pilot Knob Rd, Eagan, MN 55121. (612) 456-2349. October 4 to 6.

Buscon/88 East, New York, NY. Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500. October 4 to 6.

Electronic Imaging Conference East, Boston, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 4 to 6.

Power Electronics East, New York, NY. Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500. October 4 to 6.

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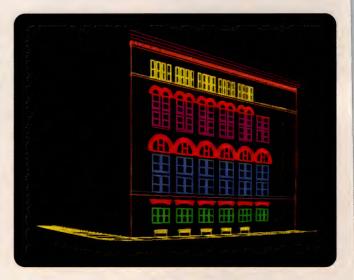
Texas Instruments TMS 34010 (2%)

AMD Am95C60 (17%)

Hitachi HD63484 (20%)

Intel 82786 (25%)

GeoCad perspective drawing courtesy of Rudolph Horowitz and Associates, Architects.
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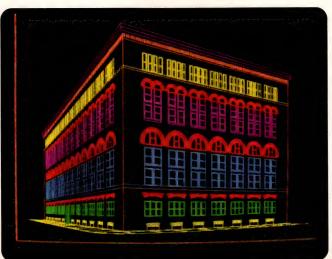
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EDITORIAL

Spend it here

A guest editorial in the June 21st *Wall Street Journal* describes the causes of today's memory-chip shortages and defends the 1986 semiconductor pact between Japan and the US. According to the author, the Japanese priced dynamic-RAM chips below cost in the early 1980s in order to drive US manufacturers out of the DRAM business. Thus, they aimed to secure the world's semiconductor markets for the Japanese manufacturers. It's true that dumping products into a market can force out domestic suppliers—as many US DRAM manufacturers found out. However, the semiconductor pact took an illogical and shortsighted approach that continues to hurt US semiconductor suppliers and consumers.

In essence, the pact forces Japanese suppliers to charge a "fair" price for their DRAM chips. However, by raising prices to artificially high levels, we give foreign manufacturers extra profit, and we fund their research. The pact gives US industries some time to regroup, but that time is hard to put a price on. As an alternative to the pact, the US could impose a tariff, but according to the *Journal's* contributor, a tariff would result in immediate shortages—although the author doesn't explain why. Also, multinational companies could circumvent any tariff by purchasing low-cost DRAMs in overseas markets where tariffs don't exist.

In most cases, tariffs are counterproductive—companies use them as a shield against foreign competitors. After all, if the government forces up the price for a commodity, there's no incentive for domestic companies to increase manufacturing productivity or take any other measures to compete against low-cost foreign imports. But a short-term tariff on imported semiconductors just might work. If semiconductor prices must go up, I'd rather have the extra money stay in the US than go to fund Japanese researchers' next DRAM breakthrough.

So, let's eliminate the "fair" prices and let the Japanese and others charge what the market will bear. Then let's have the US government impose a tariff on every foreign DRAM that enters the US, whether it's in a tube of chips or in a telephone manufactured in Hong Kong. We'll set the tariff at $1 per chip.

The funds collected from the tariff will go to an industry-research group such as Sematech and to US university labs working on semiconductor research. However, a semiconductor-tariff law must have a few restrictions. First, no one will be permitted to license or transfer any of the tariff-funded research information or process technology to a foreign-owned or -dominated company. Second, the tariff will diminish to zero over the next two years, and it won't be reimposed. If we detect dumping again, however, a tariff will go into effect again. To get the ball rolling, I'll contribute $1 for every foreign-made DRAM chip in my PC—even though I bought them before the dumping started. Just tell me where to send the check.

Jon Titus
Editor

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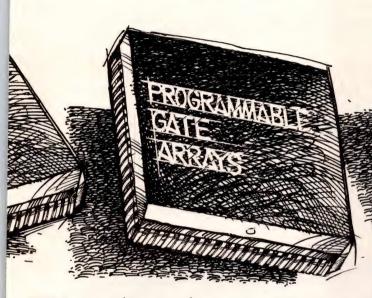
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TECHNOLOGY UPDATE

Third-party PC graphics packages streamline your programming tasks

Margery S Conner,
Regional Editor

Attention-grabbing, colorful graphics can dramatically enhance the software you write, regardless of whether you're developing it for your company's internal use or for customers. When you're writing software for IBM PCs and compatible computers, however, you'll find that addressing the PC's graphics hardware is a difficult task. To lighten your programming chores, consider using third-party graphics-software packages.

Third-party graphics packages for PCs come in varying degrees of complexity. Many are simply libraries of graphics subroutines that you'd otherwise have to write yourself. These packages range from general-purpose libraries (often called graphics toolkits), to libraries of specialized scientific subroutines. Other third-party packages include a graphics editor that helps you develop your display format in a hurry, and a complex graphics platform that offers a complete graphics-programming environment. By taking advantage of any these packages, you can develop graphics displays faster and for a wider variety of display adapters than you could on your own.

Until recently, most C and Pascal compilers for the IBM PC provided minimal support for color graphics displays. Third-party packages have filled that graphics void. However, since EGA and VGA adapters —with their relatively high resolution—have become commonplace, the compiler vendors have beefed up the graphics libraries available with their compilers.

Borland International (Scotts Val-

Although the Halo '88 graphics library explicitly supports only 2-D renderings, you can develop 3-D renderings with it. Mega CADD (Seattle, WA) used Halo '88 as the graphics library for its Mega CADD 3D, a CAD software package.

ley, CA), for example, which sells two of the most popular versions of C and Pascal, now also offers the Borland Graphics Interface (BGI). BGI is a common graphics interface: Whether you're programming in Borland's Turbo C or Turbo Pascal, the graphics library is the same. A further advantage of using BGI is that if you're developing software for resale, you don't have to pay a royalty fee, as you do when you use most of the third-party packages for that purpose.

Keep in mind, however, that BGI is essentially just a library of primitives, which are the basic graphics commands, such as the commands to draw a point, line, circle, and polygon, and the commands to fill a circle and a polygon. Third-party graphics packages not only offer more-elaborate graphics commands, but also give you the option of programming in coordinates other than Cartesian ones. (Cartesian coordi-

nates are specific to a particular display.)

Toolkits complement compilers

If your compiler already includes a good amount of graphics support, the complexity of your application's graphics will determine whether you'll need to lay out the extra money for a third-party graphics package. Chuck Batterman, graphics manager for Borland, explains: "If you don't need the high-level windowing and world coordinates supplied in the third-party packages, then BGI will do the job for you. And if you do need the more exotic graphics, then you can get your feet wet with the BGI and know that the third-party system is a reasonable investment." In other words, if you don't know whether you need a third-party package, you can find out by using the graphics supplied with your compiler to create a prototype of your display.

TECHNOLOGY UPDATE

Halo '88 from Media Cybernetics, for example, gives you the choice of specifying graphics positions in Cartesian, world, or normalized world coordinates. Unlike Cartesian coordinates, world coordinates are not specific to a particular display. Normalized world coordinates are world coordinates expressed as a number between zero and one.

World coordinates are useful when your software may have to run on a variety of graphics boards, because display coordinates vary from one board to another. If you use Cartesian coordinates, you must know the resolution of each supported graphics device, and your software won't be device independent. With Halo '88's implementation of world coordinates, you specify the resolution of the graphics, and Halo '88 maps the coordinates in your program to the device coordinates of your display adapter.

Because the compilers' graphics libraries have graphics drivers that access the EGA and VGA boards directly through the hardware, they are not device independent. Device independence allows a graphics program developed for one board—say, a nonintelligent EGA—to run on another board, such as an intelligent graphics-coprocessor-based board. When you use a device-independent program, you can specify your system's board at run time, and the program will then automatically send the correct level of information to that board. For the EGA, for example, the software must calculate the position of each pixel; for a board based on Texas Instruments' (Houston, TX) TMS34010, the software only needs to send the graphics primitives.

Third-party packages support a wide range of EGA and VGA boards that offer resolutions beyond the IBM standard, as well as boards with graphics coprocessors. Halo '88, for example, supports 144 different display adapters.

Also keep in mind that the graphics libraries supplied with compilers don't support a wide range of hardcopy output devices, but third-party packages commonly support a plethora of plotters and printers.

Port software from OS/2

A third-party graphics package that provides for portability between MS-DOS and the forthcoming OS/2 is crucial for you if your software will have to run under both operating systems. The Graphics Development Toolkit (GDT) from Graphics Software Systems is available in both OS/2 and MS-DOS versions, and their source code is compatible. GDT also supports IBM's new 8514/A intelligent display adapter. Because IBM hasn't re-

REPRESENTATIVE THIRD-PARTY GRAPHICS PACKAGES FOR IBM PCs AND COMPATIBLES

MANUFACTURER	PACKAGE	MICROSOFT C	TURBO C	LATTICE C	TURBO PASCAL	RYAN-MCFARLAN FORTRAN	LAHEY FORTRAN	IBM ASSEMBLER	MICROSOFT ASSEMBLER	PRICE	NOTES
COURSEWARE APPLICATIONS INC	DRAWBRIDGE	•	•		•					$129	GRAPHICS EDITOR DETERMINES, COORDINATES, AND GENERATES CALLS FROM POSITION OF MOUSE: METAWINDOW VERSION IS $49
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GRAPHICS SOFTWARE SYSTEMS INC	GRAPHICS DEVELOPMENT TOOLKIT	•		•	•	•	•	•	•	$495	SOFTWARE THAT USES MS-DOS VERSION IS PORTABLE TO OS/2
METAGRAPHICS SOFTWARE CORP	METAWINDOW	•	•	•	•	•	•	•	•	$195	HAS DOS-RESIDENT DRIVER: BINDING-SPECIFIC VERSION FOR C COMPILERS IS $95
	METAWINDOW/PLUS	•		•			•	•	•	$275	LINKABLE LIBRARY: GENERATES .EXE FILE
	METAWINDOW/PREMIUM	•		•			•	•	•	$495	LINKABLE LIBRARY WORKS WITH INTELLIGENT COPROCESSOR-BASED BOARDS
MEDIA CYBERNETICS INC	HALO '88	•	•	•	•	•		•	•	$325	
SCIENTIFIC ENDEAVORS CORP	GRAPHIC	•	•	•						$395	MATH FUNCTIONS AND BASIC GRAPHICS PRIMITIVES

leased much information about this board's hardware, writing to it through an interface such as the GDT's is the best way at present to ensure that your software will run on the board.

Virtually all graphics toolkits must appeal to two different kinds of customers: the programmer who uses the graphics features only in programs for his or her company's internal use, and the programmer who uses the packages to develop a software-based product. Metagraphics lets you choose from three versions of its graphics package. The standard Metawindow package costs $195 and supports a wide variety of compilers for C, Pascal, and Fortran. The company also offers a version for $95 that supports either Microsoft C, Turbo C, or Turbo Pascal. Both these packages have DOS-resident drivers. Every time you run the program, you must first load the graphics driver into memory. (The driver can also be deleted from memory from the DOS level.) These programs are best for personal use or internal company use.

For $275, you can obtain Metawindow/Plus, which includes a linkable graphics library; your application program links in only the graphics functions it actually uses, and it consists of a single .EXE file. Further, the code for Metawindow/Plus is more compact than that of the DOS-resident driver version. The Plus version also supports display adapters with resolutions higher than those of the standard EGA and VGA boards. The $495 Metawindow/Premium is also linkable, and it supports display adapters that have onboard graphics coprocessors, such as the Genesis 1280 from National Design (Austin, TX), which is based on TI's TMS34010.

Down-and-dirty math library

If you're developing software that will display graphs of specialized math functions rather than using more general-purpose graphic elements, such as windows, consider
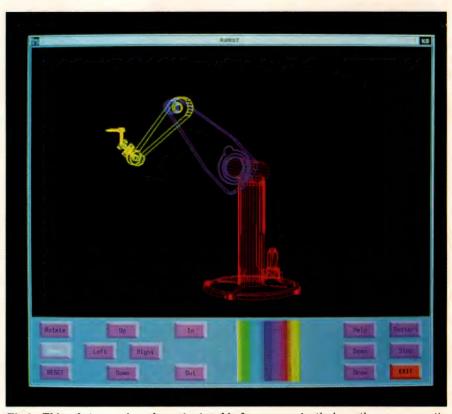
Fig 1—This robot comprises elements stored in four segments: the base, the upper arm, the lower arm, and the torch. Because of the hierarchical relationship among the elements, a command to rotate the base will cause the arms and the torch to rotate along with it. The robot was developed at Cornell University with the Hoops graphics package.

using Graphic from Scientific Endeavors. Its $395 price includes source code. The software performs all the calculations for a high-resolution Tektronix format of 4096×3120 pixels and shrinks it down to suit the lower-resolution EGA/VGA format. It stores the higher-resolution display on disk. Because most printers, even inexpensive ones, have higher resolution than the VGA's 640×480 pixels, you can print out a high-resolution hard copy of your math functions.
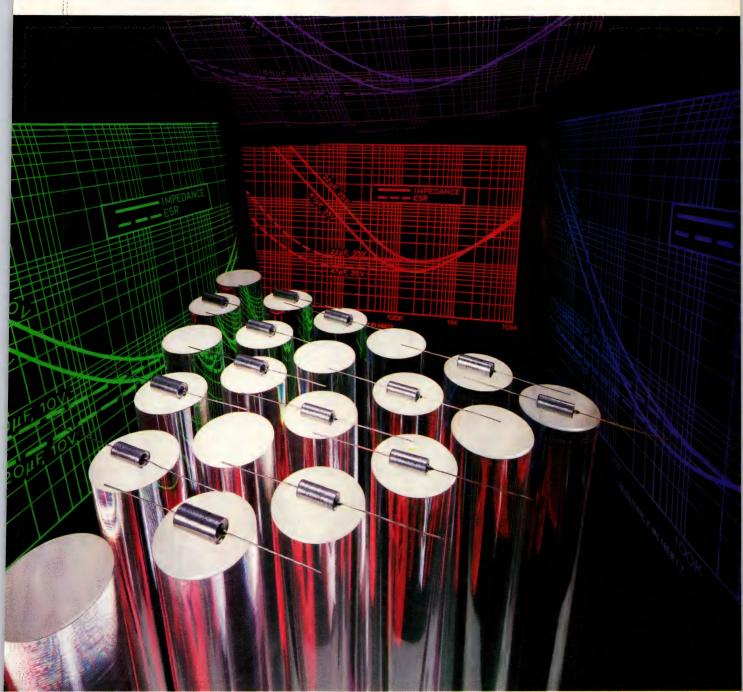
Because the functions are computation-intensive, it's best to use the Graphic package with a math coprocessor. For example, a 6-MHz PC/AT without a math coprocessor takes about 90 seconds to complete a typical plot with 600 trigonometric function calls; with a math coprocessor, it takes under 10 seconds.

With any of these graphics libraries, you still have to figure out the coordinates at which you want graphical elements such as windows

and icons to appear. This task can quickly become tedious unless you use a package such as Courseware Applications Inc's Drawbridge, a graphics editor that lets you position the elements on the screen with a pointing device such as a mouse. Once you've determined the placement of the elements, Drawbridge determines all of the coordinates and generates the library calls needed to display them. Drawbridge does not contain the subroutines themselves; instead, it acts in conjuction with a graphics library. It currently supports the Microsoft C, Turbo Pascal, and Turbo C libraries ($129 each), and the Metawindow package ($49).

If your graphics needs are complex—that is, if you require lots of transformations and 3-D manipulations—you may be able to justify using a graphics platform such as Hoops from Ithaca Software Inc. Hoops supports 2-D and 3-D rendering as well as hidden-line removal

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and shading from multiple light sources.

Most graphics libraries are procedural; they comprise many detailed, explicit drawing instructions, but have no structure that relates the various elements of the display. Hoops stores the display's graphical elements in a hierarchical database. The software lets you manipulate the display by creating the graphical elements and defining the relationships between the elements. Once you've established the relationships between the elements, you can modify the image (change the perspective, say) with just a single command.

The database's basic units are segments, or named places in the database where you can store related primitives. You create a graphics element by grouping the primitives that describe the element into a segment. Then you use declarative commands to define which elements in the database will be displayed, where they'll be displayed, and how they'll be rendered (in other words, what attributes they'll have, such as color or pattern).

The primitives in a segment are drawn according to the attributes set within the segment. Because the segments are related hierarchically, if a segment doesn't specifically set the attribute, it inherits the attribute setting from the segment that precedes it in the hierarchy.
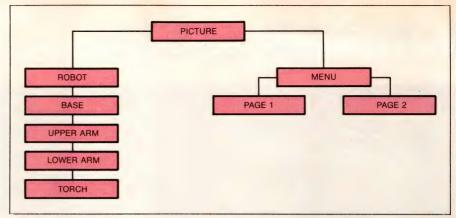
The robot in **Fig 1** provides an illustration of this characteristic. The display shows both the robot itself and a selection menu. As you can see from **Fig 2**, the robot figure breaks down into four components: the base, the upper arm, the lower arm, and the torch. The primitives used to draw the lower arm, for example, are stored segments corresponding to that component. The color attribute is set to yellow. The segment under the lower-arm segment contains the primitives for drawing the torch. You don't have to specify the yellow color again for the torch, because it will inherit that

attribute from the lower-arm segment.

Note that the robot is 3-dimensional, and the menu and icons on the screen need only two dimensions. If you just set the z axis to zero, any movement or manipulation of the menu portion of the display will still involve the z axis, even though it's set to zero. You can eliminate the z axis for just the menu portion of the database; any lower segment inherits the absence of z.

Hoops defines an element's coordinates on an even more abstract level than the toolkits do: Hoops gives the graphical element's position in relationship to the scene's other graphical elements. For example, under a conventional graphics library, if you point to a spot on the screen with a mouse and query the mouse's position, you'll receive an answer in x-y-z coordinates. If you query Hoops, its response would be, say, "on the torch tip," or "the bottom of the lower arm."

For a small program—a few hundred lines of code—Hoops may be a little faster than a toolkit such as GDT, Halo '88, or Metawindow, but you probably wouldn't want to spend the time learning to program in the Hoops environment. For programs of 1000 to 1 million lines, however, Hoops gives you a big advantage over a toolkit. **EDN**

Fig 2—*This tree illustrates the hierarchical relationship* among the segments of the robot in *Fig 1. Any attributes, such as color or pattern, that are set for a segment can be inherited by the segment below it.*

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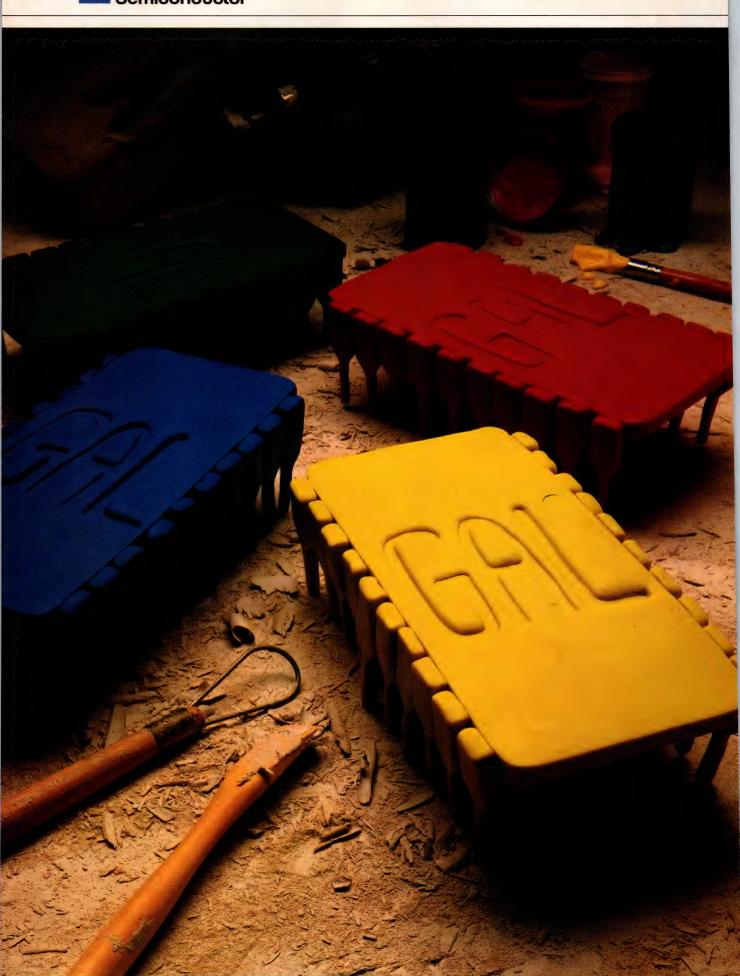
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100% Testability	no	no	yes

National Semiconductor

Limited selection of monolithic PLL ICs suffices for current applications

Tarlton Fleming,
Associate Editor

Monolithic phase-locked-loop (PLL) circuits provide an elegant way to achieve frequency demodulation or digital selection of frequency. As a result, PLL ICs have become vital components in modern TVs, car radios, frequency-shift-keyed (FSK) systems, and disk-drive electronics. You might expect, then, to find a robust market for PLL circuits.

Currently, though, domestic IC companies offer a sparse selection of new PLL devices. This lack of activity is surprising when you consider the extensive applications support that was once available to an engineer intent on designing a phase-locked loop into his system. It's doubly surprising when you consider the current emphasis on designing discrete-component PLL circuits for frequency-agile, military-RF systems. The truth is that much PLL work has moved offshore, along with the design and manufacture of certain high-volume, PLL-based products—car radios, for instance. Fortunately, enough applications remain in the US to support a continuing demand for domestically produced PLL ICs.

A PLL is a small servo system in which negative feedback forces the frequency of a voltage-controlled oscillator (VCO) equal to that of the applied signal, f_{IN} (**Fig 1**). This action causes the PLL to sense and track the f_{IN} frequency, thereby reconstructing f_{IN} and removing noise in the process (which is a form of filtering).

If you monitor the VCO's input instead of its output, the PLL will function as a frequency-sensing device suitable for FM detection or
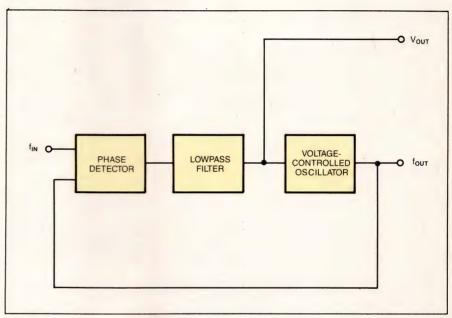
Fig 1—The basic phase-locked-loop circuit is a small servo system. The voltage output is proportional to frequency, and the frequency output is a noise-free equivalent of f_{IN}.

FSK demodulation. These two configurations (taking the PLL's output from the VCO's input or its output) account for most applications. If you add a divide-by-M counter at the input and a divide-by-N counter within the loop, at the VCO output, the PLL can also produce a digitally selectable frequency, $f_{IN}(N/M)$.

Many low-frequency applications (approximately 1 MHz and below) use the industry-standard CMOS PLL, whose generic part number is 4046. Manufacturers of this type include GE/RCA, Motorola, National Semiconductor, and Signetics. The Motorola MC14046BCP is a representative part: It costs $0.93 in quantities of 100.

The 4046 devices include two types of digital phase detectors on chip. (Most other PLLs feature one type, not both.) Your 4046 application determines whether a type I or type II phase detector is most ap-

propriate, and you then make external connections for including that detector in the loop.

Type I vs II phase

The type I phase detector is simply an XOR gate. The output signal, after passing through an external lowpass filter, produces a linear ramp in which the amplitude is proportional to the phase (0 to 180°) between f_{IN} and the onboard VCO signal. The ramp reverses and repeats when the PLL is out of lock, forming a sawtooth waveform. The type I phase detector provides the widest lock range (the f_{IN} range for which the loop will remain locked) for input signals with a duty cycle of 50%. When the loop is locked at the VCO's free-running frequency, the phase detector generates a dc level at half the ramp amplitude—equivalent to a 90° phase difference.

If nonzero phase in the locked condition is unacceptable, you can

use the type II (edge-controlled) phase detector, which ignores waveform duty cycles by operating on the two input signals' positive-going digital edges. While in the locked condition, the phase detector allows no phase difference between the VCO and f_{IN} signals. The type II detector provides a large capture range (the range of f_{IN} for which an unlocked PLL can achieve the locked condition) that is independent of the external filter's time constant.

When unlocked, the detector produces a high or low dc level according to the relative frequency values for f_{IN} and the VCO signal (vs the ac output of a type I detector). This circuit, also known as a phase-frequency detector, was an important advance in the development of PLLs at the time of its introduction.

Exar and Signetics are noted for their PLL product lines. Exar's XR-210, for example, suits FSK applications and includes a VCO, an XOR-gate phase detector, and a voltage comparator. The device operates with a 5V supply over frequencies of 0.5 Hz to 20 MHz. Housed in a 16-pin ceramic DIP, an XR-210CN sells for $2.78 (100).

The more-complex XR-2211, second-sourced by Raytheon, also fits data-communications tasks such as tone decoding and FSK demodulation. The 2211 has an analog-multiplier-type phase detector (Gilbert cell) that subtracts the two input signals. It provides outputs for lock detection and FSK demodulation, and it operates from 0.01 Hz to 300 kHz. Exar's version costs $2.89 (100).

For applications that require temperature stability, Exar's precision XR-2212 PLL operates from 0.01 Hz to 300 kHz and exhibits a 20-ppm/°C temperature coefficient of the VCO frequency. The XR-2212 comes in a 16-pin DIP and costs $2.88 (100).

Signetics uses a bipolar process in its high-frequency NE568 design in which the f_T for the npn transistors

exceeds 6 GHz. The result is a 150-MHz PLL suitable for incorporation in satellite receivers, fiber-optic video links, and VHF-range FSK demodulators.

Realizing that proper pc-board and component layout is essential at high frequencies, Signetics includes an evaluation circuit with the NE568's data sheet, as well as a pc-board pattern and parts list. According to the manufacturer, with a good layout and surface-mount capacitors, the device demodulates ±10% deviations from a 70-MHz IF and exhibits a linearity error of less than 4%. An NE568N comes in a 20-pin DIP, draws 60 mA from a 5V supply, and costs $1.79 (100).

Digital vs analog PLLs

Although overwhelmingly digital, most PLL ICs are called analog PLLs because their VCO input is an analog error voltage. The SN74LS297 from Texas Instruments, however, is all digital. The device has a counter and increment/decrement circuit in place of the conventional lowpass filter and VCO. To program the counter, you use a 4-bit digital word, which corresponds to setting the filter time constant in an analog PLL circuit. (Both types of adjustments tradeoff

loop bandwidth and phase jitter.) The SN74LS297's operating-frequency range is dc to 50 MHz. A 16-pin, plastic-DIP version costs $11.69 (100).

Unlike the discrete-IC PLLs discussed so far, Sierra Semiconductor's PLL34M exists only as a CMOS cell in the vendor's semicustom-ASIC library. This standard-cell PLL circuit operates at 30 MHz (or as high as 60 MHz, with tweaking by the manufacturer). It includes a phase detector, I/O drivers, and a bandgap reference for setting the VCO frequency. The chip area is 3224 mils^2. By combining the PLL334M with other cells in the library—you have a choice of 250 digital, 50 analog, and 20 EEPROM cells—you can configure an ASIC suitable for use as a data separator in disk drives, for example. You can buy a PLL34M, plus 500 logic gates, enclosed in a 44-pin surface-mount package for $3.50 (100,000).

Prescalers offer alternatives

Siemens combines its PLLs with appropriate prescaling circuits to produce ICs capable of handling the high frequencies involved in digital channel selection in TVs and radios. These products are partial PLLs because they operate in conjunction

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For more information . . .

For more information on the PLL products discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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with an external tuning chip that contains the VCO. Model SDA 3202-2, for instance, includes an RF amplifier, a phase-frequency detector, and a serial-data µP interface. Counter circuits on the chip can scale signal frequencies as high as 1.3 GHz. The phase detector then compares the result with a 7.8125-kHz reference (obtained from an onboard oscillator divider and an external crystal). In an 18-pin DIP, the device draws 55 mA from a 5V supply. It's priced at $4.63 (100).

Siemens uses the same approach in its SDA 2121, a device that helps provide digital tuning in AM and FM radio receivers. The CMOS chip can accept a VCO input as high as 35 MHz (AM) or 150 MHz (FM). It comes in a 20-pin DIP and costs $5.14 (100).

Similarly, the TBB 200 is a CMOS PLL circuit optimized for use in µP-controlled mobile telephones and radios. When added to an external VCO tuner and prescaler, the chip forms a compact system suitable for use in circuits operating above 900 MHz. The TBB 200 comes in a 14-pin DIP and costs $5.61 (100).   **EDN**
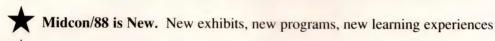
**Article Interest Quotient
(Circle One)
High 512 Medium 513 Low 514**

Video and system controller IC promises low-cost 16/32-bit color computers

Used in conjunction with the company's 68070 μP, the 66470 video and system controller IC allows you to build a complete 16/32-bit processing and color display system, using as few as 10 ICs. You can also utilize the device with other 68000-family μPs. The 66470 incorporates a dynamic RAM controller for video/system RAM, display control logic, a pixel accelerator, and an interface for an optional graphics coprocessor. Its system-controller functions include reset frequencing, address decoding, interrupt, DTACK generation logic, and a watchdog timer.

The dynamic RAM controller supports dynamic RAMs with capacities as high as 1M bit, and the address decoding provides chip selects for as much as 1.5M bytes of video/system RAM, 0.5M bytes of ROM, and 1k byte of peripheral I/O space. You can configure as much as 1M byte of the RAM as video memory, containing 4- or 8-bit pixels to provide 768×560-pixel 16-color, or 384×280-pixel 256-color displays, respectively. Lower screen resolutions are also possible. You can program the video start address anywhere within the 1M byte of video RAM; each screen pixel occupies either a nibble or a byte in memory, thus simplifying the fetching of pixel information for modification by the system's CPU or the 66470's pixel accelerator. You can configure the video RAM for logical or physical screen modes and generate either full screens or screens with a programmable border color.

The video-display logic provides a digital output for use with an external D/A converter or color look-up table. The display timing is compatible with European, Japanese, and US standards for TV and Teletext.

Using the 68070/66470 chip set, this single-Eurocard board contains all the components required to implement a 16/32-bit color computer, and still has room to spare.

You can synchronize the 66470 with a TV signal or with another 66470, and a RAM-control mechanism allows you to operate the video RAM as a frame grabber.

Associated with the video RAM are two areas of memory that contain instructions to control the display. The first of these, designated the image control area (ICA), is accessed before the start of each frame—that is, during the display's vertical retrace period. The second area, designated the dynamic control area (DCA), contains as much as 64 bytes of information for each horizontal line in the display. The instructions in the dynamic control area for a particular display line are fetched and executed during the horizontal retrace period that precedes the display of that line.

The ICA/DCA instruction list in-

cludes instructions to reload the video start address, generate a processor interrupt, and change the border color. You can also include instructions to control a back-end processor that's connected to the video output port. The ability to change the video start address on a frame-by-frame or line-by-line basis allows you to achieve a variety of special effects, including horizontal and vertical smooth scrolling, or division of the screen into a number of horizontal subscreens.

To manipulate individual pixels in the image, you can use the 66470's on-chip pixel accelerator rather than the system CPU. This accelerator can perform pixel operations in a single instruction cycle that would take several instruction cycles if you performed them using the 68000's instruction set. Operations that the

pixel accelerator can perform include copying source pixels to destination pixels, exchanging source and destination pixels, transferring source pixels to destination pixels with an associated color change to the current foreground or background color, changing pixels to the current foreground or background color according to a bit-map, and testing pixel color.

You can make most of these operations conditional on whether or not the source pixel's color coincides with the currently defined transparent color. Other pixel accelerator operations, which can execute concurrently with some of the operations described above, include horizontal zooming or shrinking of the display by a factor of 2, transparency test inversion, and a range of logical operations on the result of the pixel operation.

The pixel accelerator doesn't operate as a coprocessor that needs to take control of the CPU's address and data bus. Instead, you use the CPU to set up the required pixel operation in the pixel accelerator, then use the CPU to move data to and from registers in the pixel accelerator. The pixel accelerator is automatically triggered to perform the pixel operation when the CPU writes data to the appropriate register.

To further speed image manipulation, you can program the pixel accelerator to operate with implicit addressing. In this mode, the appropriate register in the pixel accelerator is automatically connected to the dynamic RAM's data bus when the CPU reads or writes data from or to memory. As a result, you can execute many pixel operations with a single 68000 move instruction. In addition to controlling the pixel accelerator from the system's main CPU, you can also control it via the 66470's coprocessor interface.

The 66470 is a CMOS part that operates from a single 5V supply and draws a maximum operating supply current of 65 mA at a clock frequency of 30 MHz. It is packaged in a 124-pin quad flatpack, surface-mount package. Initial samples of the 66470 have been implemented in a gate array and are available at a cost of around $50 (100). The company expects that full custom parts with enhanced functionality will be available in 1989 at a cost of around $25 (100), but that a high-volume price for the 68070/66470 chip set will be around $30 by 1991.
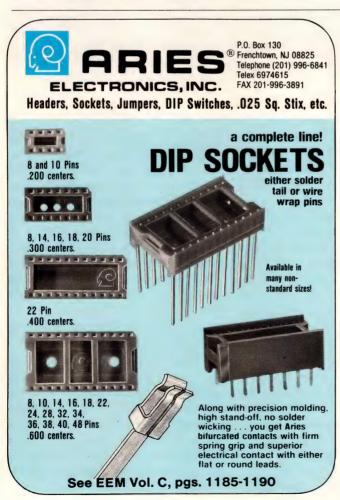
—Peter Harold

Philips, Components Division, 5600 AM Eindhoven, The Netherlands. Phone (040) 757189. TLX 51573.

Circle No 726
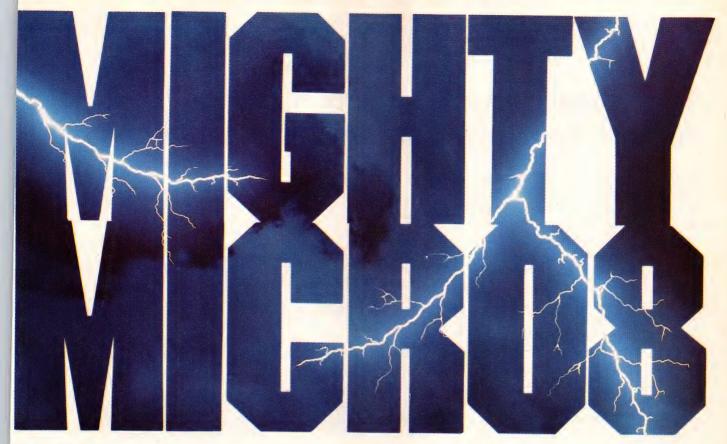
Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-4571.

Circle No 727

Data logger acts as system analyzer in both benchtop and field environments

If your embedded-control application includes the 6800 or 68000 family, consider using the Step-120 Mobile Incident Logger (MIL). Although it's geared specifically for the automotive industry, the unit offers a combination of features that also make it suitable for use as a system analyzer in both benchtop and field environments.

The MIL requires an IBM PC or compatible computer to act as a host for data transfer and for initialization. Once initialized, however, the unit operates independently of the host and doesn't need to remain connected to it. Nonvolatile RAM in the unit retains the setup conditions and the acquired data, so you can use the data logger to collect data in the field as well as on the test bench.

The unit records three types of data: processor-bus data, RAM variables, and external events. You can specify match (or comparison) words for each data type, using the match words for triggering and for data filtering. When filtering, the unit stores only those samples that meet the match-word conditions. The data logger can store 32k samples, which you can configure as a single-sample memory or as four 8k-sample memories for repeated sample runs.

The bus section of the unit monitors the behavior of the processor. The unit will record a 16-bit address bus, an 8-bit data bus, and a 3-bit status bus. (You can upgrade these bus widths to 24 bits, 16 bits, and 8 bits, respectively.) In addition, you can have the unit monitor a series of RAM addresses that you've defined. The data logger then records any transactions at those addresses.

A special feature of the unit is its code-coverage mapper. This mapper

This multipurpose instrument functions as a data logger, logic-state analyzer, and chart recorder. Together with a host computer, the Step-120 Mobile Incident Logger offers a versatile tool for embedded-control applications.

records all addresses within a 64k-address range that have been accessed by a particular type of bus cycle. You can use this feature to verify that test programs completely exercise your code. You can also use it to identify frequently used sections of code, highlighting areas where improvements in code efficiency would have the greatest impact.

The data logger has four analog channels and eight event channels. The analog inputs have a selectable range of 0 to 5V or 0 to 20V; they offer 8-bit A/D resolution. The event channels work at logic voltages, but can tolerate as much as 125V continuously.

When you've collected your data, you must use the host computer to retrieve it. Once the host contains the data, you can access that data in a variety of ways. You can view the complete data record with the data

types interleaved chronologically, or you can examine only one or two data types. You can plot the analog data as a function of time. And you can view the bus activity as disassembled code or as source code from some C compilers.

The unit operates from dc power with a 9 to 16V input range, which reflects the instrument's automotive orientation. Its operating-temperature range is −25 to +65°C, and it tolerates vibration and mechanical shock. Without a host, the data logger costs $14,900 and is available for delivery within 30 days ARO.
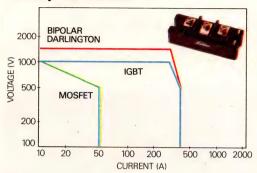
—Richard A Quinnell
Step Engineering, 661 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 733-7837.
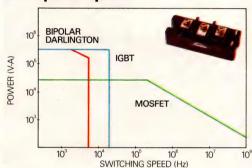
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IGBT (Insulated Gate Bipolar Transistor) Selection Guide

CIRCUIT	SYMBOL	V_{CES}(V)	MAXIMUM RATING COLLECTOR CURRENT Ic (A)									
			8	15	25	50	75	100	150	200	300	400
	BS	500		GT15H101† MG15H1BS1	GT25H101† MG25H1BS1	GT50G101† (400V) MG50H1BS1	MG75H1BS1*	MG100H1BS1				
		1000	GT8N101†*	GT15N101† MG15N1BS1	MG25N1BS1	MG50N1BS1	MG75N1BS1*					
	US	500									MG300H1US1	MG400H1US1
		600									MG300J1US1*	MG400J1US1*
		1000								MG200N1US1*	MG300N1US1*	
		1200								MG200Q1US1*	MG300Q1US1*	MG400Q1US1*
	YS	500			MG25H2YS1	MG50H2YS1	MG75H2YS1	MG100H2YS1	MG150H2YS1	MG200H2YS1		
		600					MG75J2YS1*	MG100J2YS1*	MG150J2YS1*	MG200J2YS1*		
		1000		MG15N2YS1	MG25N2YS1	MG50N2YS1	MG75N2YS1	MG100N2YS1	MG150N2YS1*			
		1200			MG25Q2YS1*	MG50Q2YS1*	MG75Q2YS1*	MG100Q2YS1*	MG150Q2YS1*	MG200Q2YS1*		
		1400			MG25S2YS1*							
	JS	1000				MG25N1JS1						
	ZS	500				MG50H1ZS1						
		1000			MG25N1ZS1							
	ES	500		MG15H6ES1*								
		1000	MG8N6ES1*	MG15N6ES1*								

†Non Isolated Type TO-3P   *Under Development

Industrial IBM PC/AT-compatible system employs an 80386 μP and 23 STD Bus slots
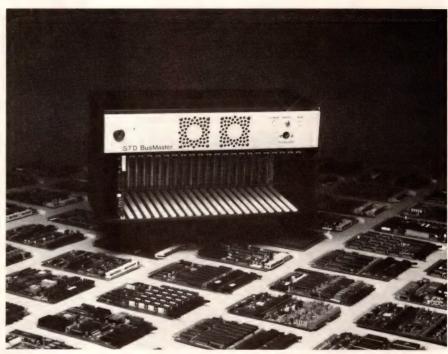
Targeting industrial-control applications, the STD Busmaster-386 system couples a 16-, 20-, or 25-MHz 80386 μP to the STD Bus. Compatible with the IBM PC/AT and MS-DOS, the system provides 23 STD Bus slots. It also includes a watchdog timer and an individual interrupt acknowledge/disable function.

The system operates in high-vibration and electrically noisy environments, and works over a 0 to 70°C temperature range. The company packages the system in an anodized-aluminum card cage that you can mount in an EIA-standard 19-in. rack or a NEMA-rated box.

To couple the 80386 to the STD Bus, the designers partitioned the system into two functional and physical sections. The 80386 μP resides on a PC/AT card that hosts as much as 16M bytes of 32-bit dynamic RAM and an optional 80387 math coprocessor. The board plugs into a passive 3-slot PC/AT-compatible mother board that is positioned in the upper portion of the card cage.

A second PC/AT-compatible board includes a video controller that is EGA, CGA, and Hercules compatible. The multifunction card includes two serial ports, a parallel port, a dual-floppy-disk-drive controller, and a SCSI host adapter. The company offers an optional ST-506 Winchester controller or LAN-controller board for the third slot. In addition, you can integrate the board of your choice in the system.

The lower portion of the card cage houses the 23 STD Bus slots and a 24th slot that interfaces the PC/AT bus to the STD Bus. A plug-in board acts as the interface between the

An 80386 μP and a 23-slot STD Bus card cage suit the STD Busmaster-386 system for industrial applications that require more computational power than typical STD Bus CPU cards offer.

two buses. The 24th slot employs a DIN connector. The 80386 can address 128k bytes of 8-bit STD Bus memory and 504 contiguous 8-bit I/O locations.

The STD Bus operates as if a 4-, 6-, or 8-MHz Z80 were the CPU. The bus-interface card passes wait states, generated by STD Bus cards, directly to the 80386. The CPU automatically inserts wait states on memory and I/O accesses to the STD Bus to emulate a Z80. You can select the STD Bus's clock frequency to be the CPU clock frequency divided by 2 or 4, or you can select it to be 7.16 or 3.58 MHz.

Eight 3-slot groups generate individually vectored interrupts that you can separately enable and disable. You can enable or disable the watchdog timer with software. You

can program timeout selection to 0.25 or 1.0 sec. The system's brown-out reset activates a system reset when the V_{CC} drops below 5 or 10% (the percentage is software selectable) of the nominal inputs.
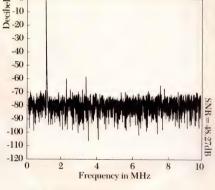
The company offers models for MS-DOS version 3.3; Unix-386 System V; Xenix System V; and QNX, a real-time version of Unix. The company will offer 8088- and 80286-based systems and a system with only eight STD Bus slots. A 16-MHz model with no DRAM installed, a 23-slot card cage, and MS-DOS costs $3995. Delivery, stock to 90 days.—*Maury Wright*

Computer Dynamics Sales, 107 S Main St, Greer, SC 29651. Phone (803) 877-8700.

Circle No 731

THE THRILL OF DESIGNING A/D SUPPORT CIRCUITRY ENDS IN A FLASH.
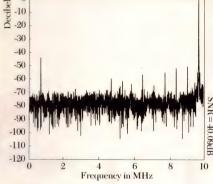
The thrill of designing voltage references, input buffers, timing, and adjustment circuitry is gone. We do it for you. And in hybrid

FFT of HS1068 Flash Converter,
Fin = 1.123MHz, Fsample = 20MHz

SNR = 48.27dB

FFT of HS1068 Flash Converter,
Fin = 9.678MHz, Fsample = 20MHz

SNR = 40.09dB

Naturally, we test each device to ensure maintenance of SNR as input frequencies climb. They'll be distortion-free in your

packages smaller than you'd expect for flash converters alone.

hypersensitive DSP applications.

Consider these three "pop-in" converters. Our 8-bit HS1068 flash A/D samples at 20MHz minimum, has no spurious or missing codes, aperture jitter of only 60ps, and true 1/2 LSB 8-bit 47dB signal-to-noise ratio. Our 8-bit SP1070 samples at 25MHz minimum and requires only 1W of power. And our dual-flash SP1072 provides the performance of two SP1070s while saving you considerable real estate.

And, we are the only company you can rely on to deliver full MIL-STD-1772 and MIL-STD-883C, self-contained, hybrid flash converters off the shelf. For data sheets, or a copy of our 382-page 1988 catalog, write SIPEX Corporation, Six Fortune Drive, Billerica, MA 01821, or call 1-800-272-1772. In Massachusetts call (617) 663-7811.

Sipex Corporation
Hybrid Systems Division

SIGNAL PROCESSING EXCELLENCE

Digital scope simultaneously captures data from two sources at 500M samples/sec

When Tektronix engineers set out to design the Model 2440 digital-storage oscilloscope, the company was concerned, of course, with performance and price. But equally important was ease of use; using the scope had to feel natural to people accustomed to using high-performance analog scopes. The result is a product that looks and acts much like a familiar analog instrument, yet provides many more features and operating conveniences. According to Tektronix, it offers the industry's highest real-time sampling rate—500M samples/sec.

The instrument's predecessor, the Model 2430A, which the company will continue to sell, has achieved a high degree of acceptance. The 2440 has the look and feel of the 2430A, but its 300-MHz vertical bandwidth improves on the earlier model's bandwidth by a factor of 2; its ability to take 500M samples/sec betters its predecessor's ability by a factor of 5; and its greatest sweep speed (2 nsec/div in equivalent-time-sampling mode) is faster by a factor of 2.5. (In real-time sampling mode, the 2440's 100-nsec/div max sweep speed is 5 times that of the 2430A.)

Moreover, the 2440 sacrifices none of the 2430A's performance. The simultaneous sampling of two inputs, 8-bit resolution, 2-mV/div max sensitivity (200 µV/div in average mode), and 1024-point record length are unchanged, as are the 6.3×13×18.9-in. dimensions and the 24-lb weight. Furthermore, the cost of the 2440 is only 29% more than that of the 2430A.

Its conveniences include auto setup that automatically configures the sensitivity and sweep speed to let you see the waveform at the input you select in the mode of your

The front panel of the 2440 digital-storage oscilloscope intentionally resembles those of high-performance analog scopes, because market research has indicated that users want scopes whose operation is intuitive to them.

choice. Auto pass/fail testing allows you to define a waveform envelope. You can then operate the scope unattended, and if any waveform falls outside your predefined envelope, the scope will store it and record the time at which it occurred. An auto-measure mode can, among other things, provide a numeric display of 20 parameters of a captured waveform.

The scope's dual timebases provide many display modes. For example, you can delay the A or B sweeps by a number of B-trigger events that you select (2^{16} max). You can also supply your own sampling clock with a frequency from 1 to 100 MHz. A glitch-capture feature enables the scope to recognize pulses that are 2 nsec wide at the 50% amplitude points (at *any* sweep speed—with 85% probability). Ex-

cept at the highest sweep speed, such pulses could fall between samples.
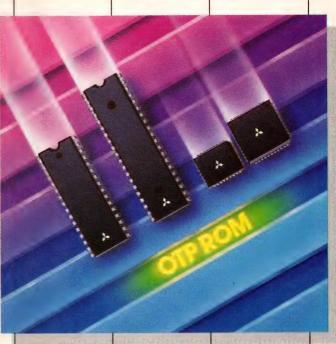
Among the unit's interfacing features is an IEEE-488 port that can send waveforms, cursor measurements, and instrument configuration to a company HC 100 color pen plotter, an HP 7400 Series plotter, or an HP Think-Jet printer. A rear-panel output also provides an analog representation of the channel-2 waveform. The price of the 2440 is $11,500, and the 2430A costs $8900.

—Dan Strassberg
Tektronix Inc, Box 1700, Beaverton, OR 97075. Phone (800) 426-2200.

Circle No 725

Modular 1500W power system suits fault-tolerant designs

By using the 29D Series modular power supplies with the company's Powersystem enclosures, you can implement 2-, 4-, or 6-supply fault-tolerant subsystems. The supplies' power ratings range from 225 to 300W. A 6-supply fault-tolerant subsystem can provide 1500W. When used in parallel, the supplies feature automatic load sharing. The family of products targets applications in telecommunications, data communications, and computer systems.

To implement a fault-tolerant subsystem, you simply connect one more supply than you need. For example, six 300W supplies actually provide 1800W in parallel, but only provide 1500W when a supply fails. The company offers isolation diodes for failed supplies, and the enclosures allow for "hot plug-in"—in other words, they let you replace a supply without taking the system off line.

The supplies provide five isolated floating outputs with voltages ranging from 5 to 24V dc. The first output supplies 5V and 30 or 40A. Outputs 2 through 5 offer combinations of 5, 12, 15, and 24V.

The supplies meet all domestic and international safety standards. They require 110 or 220V ac input power, which is field selectable. You can adjust the first four outputs to ±5% of the nominal output voltage. The fifth output tracks the first output. The supplies' line regulation is ±0.2% on all outputs. The first four outputs provide ±0.2% load regulation. The semiregulated fifth output features a ±5% load regulation. A step-load change or a 25% shift in rated maximum load causes an output change of less than 3%. The output recovers to within 1% in less than 400 μsec.

Six modular power supplies in parallel implement a 1500W fault-tolerant subsystem when mounted in the Powersystem enclosure. The enclosure offers "hot plug-in" capability; that is, it lets you replace a supply without taking the system off line.

To create fault-tolerant subsystems, you can connect the supplies in parallel. You can parallel the first output of a supply only with the first output of another supply. However, you can parallel outputs 2 through 4 within the same supply or with outputs from other supplies—as long as the outputs have equal voltages and polarities. When connected in parallel, outputs 1 through 4 share current proportionally within ±10% of each output's 50°C current rating (for forced-air cooling). You can't use the fifth output for parallel connections.

The enclosures are 7 in. high and 17½ in. deep, and the widths vary: The 2-, 4-, and 6-supply units are 5.7, 11.3, and 19 in. wide, respectively. A supply with isolation diodes and outputs of 5V/30A, 12V/3.75A, 12V/2.25A, 24V/3A, and 12V/2.25A costs $508 (25). The enclosures range from $158 (25) for a 2-supply unit to $484 (25) for a 6-supply unit. Both the supplies and the enclosures are available from stock.—*Maury Wright*

Bonar Powertec, 20550 Nordhoff St, Chatsworth, CA 91311. Phone (818) 882-0004. TLX 277483.

Circle No 730

LET THIS NEW MODEM CHIP MAKE LIFE EASY FOR YOU

The Only 5-Volt, 2400 BPS, 1-Chip Modem For Low-Power Applications

If modem chips have a place in your company's products, here's how a new low-power single-chip modem from Silicon Systems can make life easier for everyone.

Now your product designers can put this new 1-chip 2400 BPS modem into their designs and replace three or more old-style modem IC's. The K224L draws less than 120 mW from a single 5-volt supply, eliminating the need for additional power supplies and making integration of the modem function possible in lap-tops, portable terminals, and other battery-operated applications.
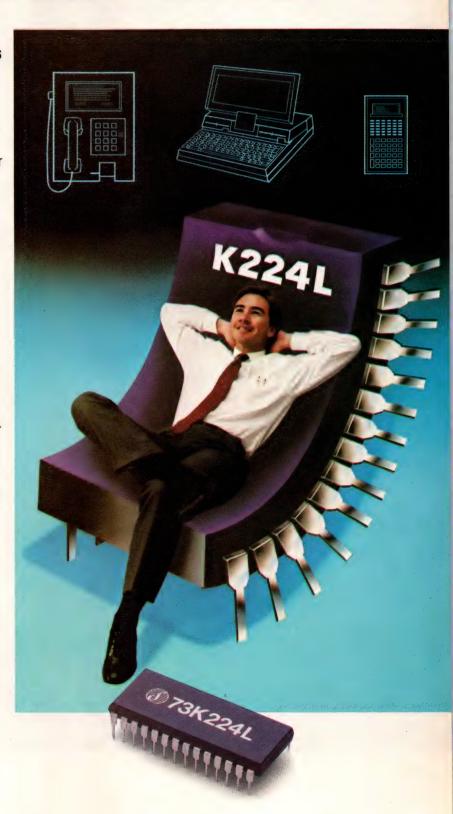
Your marketing department will be happy to know that this single chip fully supports all the world-wide operating modes—V.22 bis, V.22, V.21, and Bell 212A/103. They'll like the competitive edge that state-of-the-art single-chip modem technology can give to your company's products.

And, of course, your management team can only be proud of an engineering and marketing group that has the good sense to make the most of such innovative components that enhance the features of your products, reduce costs, and boost company sales.
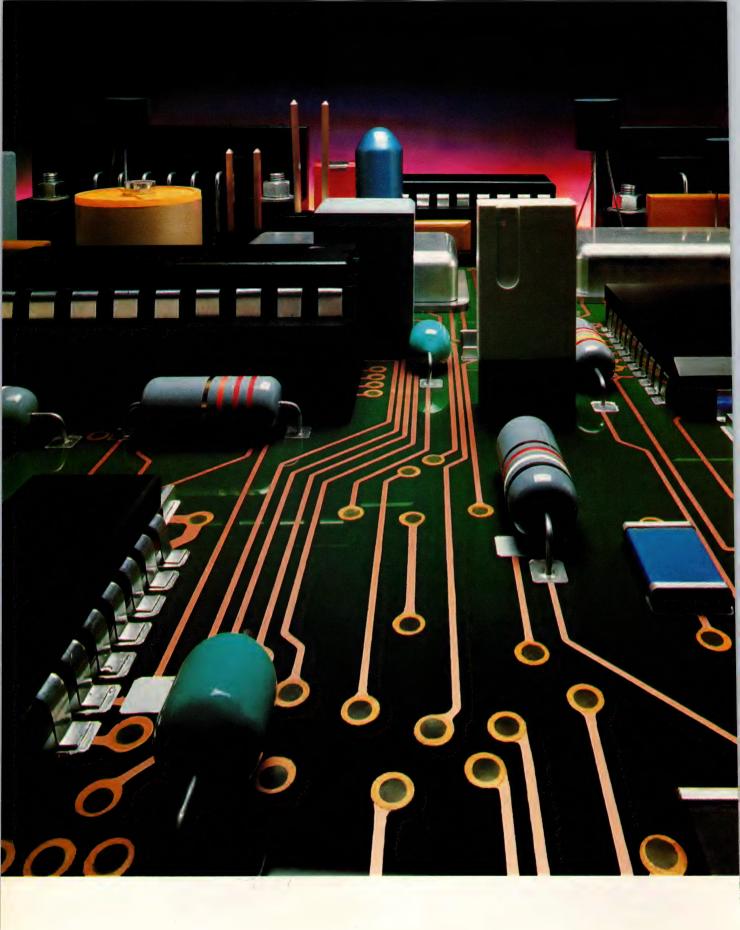
Call Now!
(714) 731-7110, Ext. 3575

For more information on the new Silicon Systems 73K224L, or any of SSi's fully compatible K-Series 1-chip modems, contact: **Silicon Systems**, 14351 Myford Road, Tustin, CA 92680.

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READERS' CHOICE

Of all the new products covered in EDN's **May 12, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, refer to the indicated pages in our **May 12, 1988,** issue, or use EDN's Express Request service.

◀ RACK-MOUNT PC/AT

The QPC-7000 IBM PC/AT-compatible computer meets EIA standards for mounting in a standard 19-in. rack (pg 244).
Qualogy Inc.
Circle No 603

TURBO C DEBUGGER

The A-COM debugger is a full-screen, source-level debugger for use with Borland International's (Scotts Valley, CA) Turbo C programming tools (pg 276).
A-Com.
Circle No 605

▲ CMOS EPROMs

The 27F64 and 28F256 flash memories are 64k-bit and 256k-bit devices, respectively, that feature in-circuit electrical erasing and reprogramming (pg 88).
Intel Corp.
Circle No 601
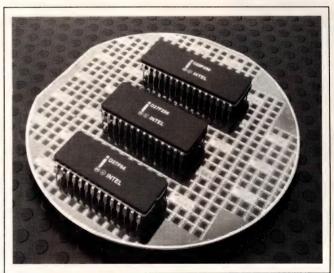
▲ 3¾-DIGIT DMM

The DM79 can provide 10 times the resolution supplied by 3½-digit meters on many measurements (pg 258).
Beckman Industrial Corp.
Circle No 604
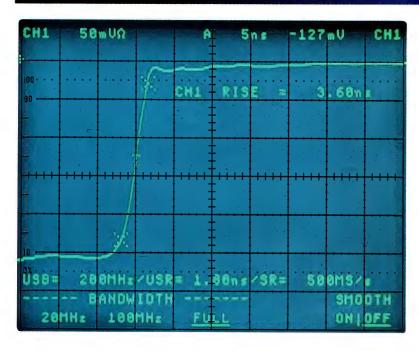
5-YEAR BATTERY

The Model PS-1242 is a 12V, sealed lead-acid battery. It's maintenance free, rechargeable, usable in any position, and suitable for both standby and deep-cycle applications (pg 243).
Power-Sonic Corp.
Circle No 602

NEW 500 MEGASAMPLES/SEC 300 MHz DIGITAL PORTABLE
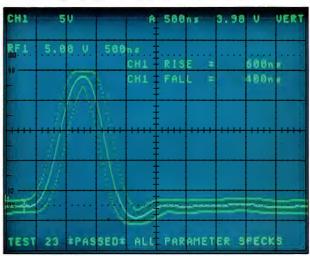
TEK PUSHES THE LIMIT...
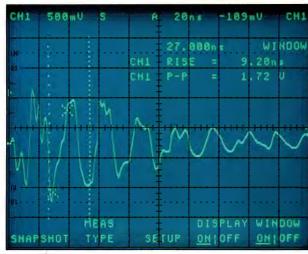
AT THE PUSH
OF A BUTTON.
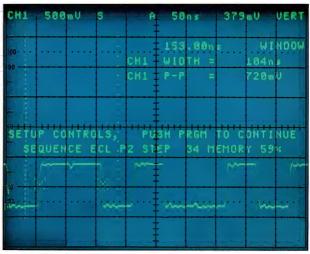
AUTO SETUP

AUTO PASS/FAIL

AUTO MEASURE

AUTO SEQUENCE

ONLY FROM TEK.

The new Tek 2440 Digital Oscilloscope is the only portable offering a 500 MS/s sampling rate—on *two* channels simultaneously.

Capture signals competitors can't.

You can digitize, store and process single-shot phenomena to 200 MHz and repetitive signals to 300 MHz. At the touch of a button.

This is a scope built for solving tough problems fast.

Complete confidence in results.

Exclusive Tek digital features let you capture glitches as short as 2 ns with continuous sampling; automatically catch intermittent failures in babysitting applications; and see waveform changes virtually as they occur thanks to the high update rate.

With the 2440's 500 MS/s sample rate, 8-bit vertical resolution, and 0.0015% crystal-controlled timebase accuracy, you'll have complete confidence in the accuracy of your waveform data. You'll know what you're seeing is what's actually happening in your circuit.

The 300 MHz 2440 and 2432, along with the 150 MHz 2430A, drive like the scopes you're used to. They feature a familiar front panel and simple, one-level menus.

Built-in automation simplifies operation even more. The scopes set up at the touch of a button. And you can characterize waveforms instantly: press another button and read out your choices from 21 different measurements.

A digital family you already know how to use.

On the design bench, the 2400 DSOs are effective standalone test systems. Full GPIB programmability, pass/fail testing and time-saving measurement sequencer make them equally powerful system components. With off-the-shelf software you can fully automate measurements and extend waveform analysis.

Don't settle for less. Get the total performance package only Tek delivers, feature for feature, spec for spec.

Powerful system components.

WHEN THE MEASUREMENT COUNTS, COUNT ON TEK.

No matter what you measure, Tek measures best.

The standard of excellence in portable scopes.

Analog or digital, standalone or automated, no other portables match Tek 2400 Series Oscilloscopes for sheer breadth of line, range of performance and wide choice of options.

Their proven reliability and built-in versatility are a result of Tek's dedication to superior waveform acquisition tailored to individual needs.

Answers at the touch of a button.

Six four-channel analog oscilloscopes combine pushbutton simplicity and leading-edge performance. They bring unprecedented efficiency to your design lab, production line or field service site.

The top-of-the-line 2467 with Tek's patented microchannel plate CRT even makes single-shot pulses to 350 MHz visible— at the touch of a button.

A complete range of options further extend each scope's capabilities.

Scope for scope, feature for feature, Tek has the best solution for your measurement needs.

Ask your Tek representative for a demonstration. With the 2440 joining the family, there's an even better selection—in sample rate, performance and price. For more information, please return the reply card or call Tek direct: **1-800-426-2200.**

Call Tek for details.

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COMMITTED TO EXCELLENCE

Our networks give more for less... less space, less time, less cost.

Mepco/Centralab thick-film networks save space and design time in all of your circuits — computer, communications, military, automotive, industrial control and instrumentation.

Choose from our broad range of highly integrated standards — cost-effective conformal networks, EMI/RFI networks, ECL terminators, MIL-R-83401 networks, capacitor banks, and more. We can also custom-design a space-saving unit to meet your requirements, including MIL designs.

With quality-designed Mepco/Centralab networks, you get the extra advantage of ordering just one part instead of many discrete components. So you simplify your purchasing, handling, stocking and assembly operations. And, since you only have to install a single part that's 100% pre-assembled and tested, you automatically improve your system's electrical and mechanical performance, and its overall reliability.

Look into space-saving, time-saving Mepco/Centralab networks for your commercial, industrial and military-grade products. They're your assurance of high reliability, plus just-in-time delivery and competitive pricing.

Ask for our catalogs. Write to Mepco/Centralab — the active leader in passive components.

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A DIVISION OF NORTH AMERICAN PHILIPS CORPORATION

PHILIPS

FDDI.
From deskwork to network.
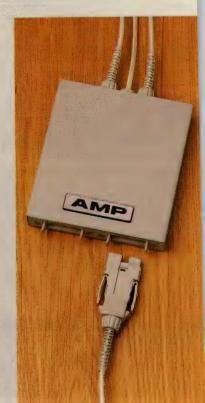
Good news for networks!

The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document.

More good news! AMP has the complete fiber optic interconnection system—the AMP OPTIMATE Fixed Shroud Duplex System—that meets all FDDI PMD requirements. And includes all the physical components you need to make your fiber optic network a reality.

Of special note: the transceiver —the first of its kind—is capable of operating at data rates up to 125 Mb/s. Available in standard or raised (+5v) ECL logic, it gives you a compact, board-mount data link in a single 24-pin module. Reliable duplex mating

and electro-optic conversion are no easier than ever.

All system components, in fact, are easy to install and reconfigure. Our field termination kit makes short work of attaching duplex connectors to fiber cable. And because all interconnections use a floating interface, you get consistent, low-loss mating (0.6 dB typical) throughout.

You can also order complete, custom-built cable assemblies from us. Either way, you'll have the assured compatibility that comes from dealing with only one supplier for all your FDDI interconnection components. A supplier whose capability in fiber optic technology is everything you'd expect from the world's largest connector company.
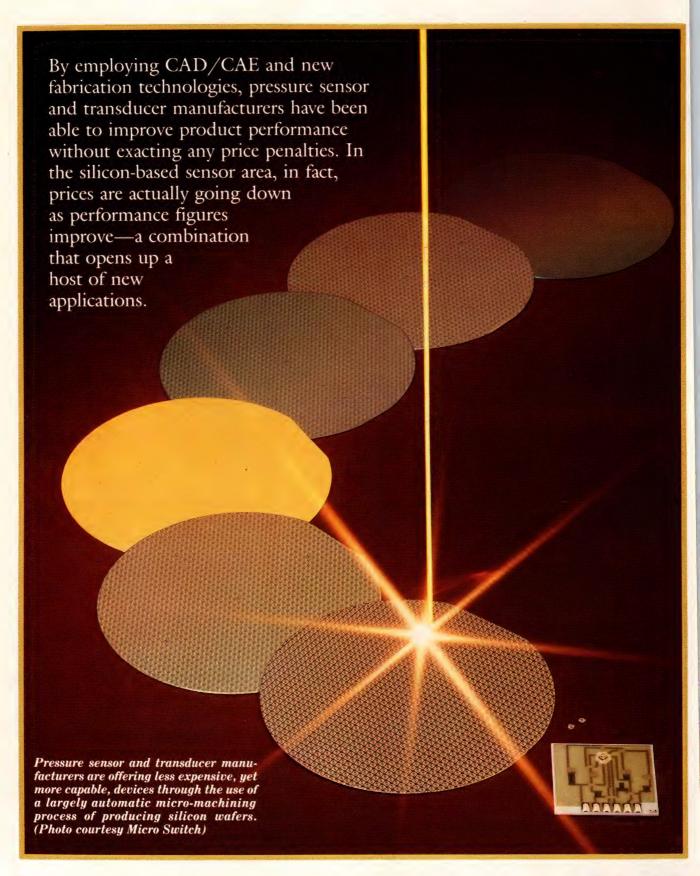
For technical literature and more information, call 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

CIRCLE NO 77

AMP Interconnecting ideas

105

By employing CAD/CAE and new fabrication technologies, pressure sensor and transducer manufacturers have been able to improve product performance without exacting any price penalties. In the silicon-based sensor area, in fact, prices are actually going down as performance figures improve—a combination that opens up a host of new applications.

Pressure sensor and transducer manufacturers are offering less expensive, yet more capable, devices through the use of a largely automatic micro-machining process of producing silicon wafers. (Photo courtesy Micro Switch)

Pressure sensors and transducers

Tom Ormond, *Senior Editor*

Improved performance at a lower cost is the ultimate goal of any product designer. When it comes to strain-gauge-type pressure sensors and transducers, manufacturers have achieved this goal and made the devices practicable for numerous applications in the automotive, medical, and military fields. In addition, advances in device-fabrication and -packaging techniques allow today's pressure sensors and transducers —including devices based on older piezoelectric and linear-variable-differential-transformer (LVDT) techniques—to easily handle the harshest industrial environments. Manufacturers are also integrating more electronics into the device package, which makes it easier for users to apply the sensors and transducers.

Amplifiers represent one type of integration. Although most of today's transducers generate usable unamplified outputs, you can get products that offer logic-level output signals while operating from low voltage supplies. Transducer manufacturers also include integral electronics that address thermal-related problems. Just about every transducer available today includes temperature-compensation circuitry, which allows the units to provide very accurate output readings in environments involving significant temperature variations. On the other hand, some manufacturers also offer uncompensated products for those users working in a benign environment, who don't want to pay for something they don't need.

Three of the most popular sensor technologies are strain-gauge (piezoresistive), LVDT, and piezoelectric. Nowadays, you'll find that most of the newsworthy technological developments concern strain-gauge types of sensors. These devices typically use one of three sensing elements: an unbonded metallic-filament strain gauge, a bonded metallic-foil strain gauge, or a bonded piezoresistive (semiconductor) gauge. Regardless of element technology, however, strain-gauge sensors and transducers find their way into diverse applications.
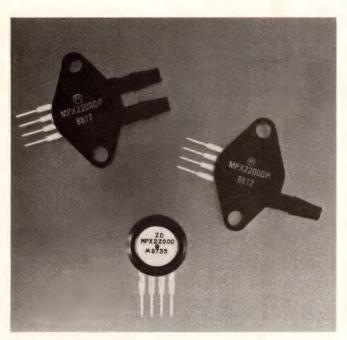
Solid-state sensors—where the action's at

Gulton Industries' GMS110 Series of pellicloid thin-film strain-gauge transducers, for instance, fit demanding military as well as aerospace applications. Packaged in a welded, hermetically sealed housing, the solid-state devices are available in versions that measure full-scale absolute or gauge pressures of 15 to 5000 psi.
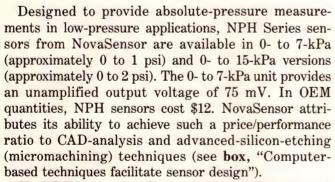
The sensors consist of a thin-film circuit deposited on a micromachined silicon diaphragm. Pressure across the diaphragm produces strain in the metal-film sensing elements, causing slight changes in their resistances. These sensing elements are configured as a 4-arm, fully active strain-gauge bridge with integral trimming resistors. The fabrication process places the compensation resistors close to the sensing elements to minimize thermal shift in the span and zero parameters: 0.005% full-scale output (FSO)/°F max.

The GMS110 Series operates from 10V dc; the transducer output is 2.5 mV/V min. Repeatability and hysteresis are 0.05% FSO max, and nonlinearity equals ±0.25% max. The overall operating range spans −320 to +350°F; the compensated range is −65 to +250°F. The transducers cost $1050.

Featuring 0.2-mV/kPa sensitivity, Motorola's MPX2000 Series temperature-compensated transducers spec ±0.05% full-scale linearity over −40 to +125°C.

Offering 1- and 2-psi FS measurement ranges, NPH sensors from NovaSensor feature maximum nonlinearity and hysteresis errors of ±0.2 and ±0.5%, respectively.

Designed to provide absolute-pressure measurements in low-pressure applications, NPH Series sensors from NovaSensor are available in 0- to 7-kPa (approximately 0 to 1 psi) and 0- to 15-kPa versions (approximately 0 to 2 psi). The 0- to 7-kPa unit provides an unamplified output voltage of 75 mV. In OEM quantities, NPH sensors cost $12. NovaSensor attributes its ability to achieve such a price/performance ratio to CAD-analysis and advanced-silicon-etching (micromachining) techniques (see **box**, "Computer-based techniques facilitate sensor design").

The NPH Series specifies respective nonlinearity and hysteresis errors of ±0.2% and ±0.05% max. Thermal hysteresis is less than ±0.25% FSO, and thermal error is 1% max over the 0 to 70°C compensated operating-temperature range. The sensors are also available in uncompensated versions, as are models that provide differential-pressure readings. All models are compatible with noncorrosive gas and moist-air media. A pressure port with an outside diameter of ³⁄₁₆ in. is standard, but similar tubes or vent holes for either TO-5 or TO-8 packages are available to satisfy specific OEM requirements.

Endevco's strain-gauge Model 8515B is a rugged, miniature transducer designed for applications requiring surface-pressure measurements. It utilizes a sculp-

tured, piezoresistive pressure-sensing diaphragm and readily mounts on curved surfaces without affecting laminar-air or hot-gas flow. For a flush fit, you can recess the transducer and lead wires into the mounting surface. The transducer includes a protective screen to protect against particle impingement.

The $495 transducer is available in full-scale versions of 15 psia (pounds per square in. absolute) (Model 8515B-15) and 50 psia (Model 8515B-50). The 0.03×0.25-in. case contains hybrid temperature-compensation circuitry that stabilizes operation over the −65 to +250°F temperature range. Full-scale output measures 300 mV. For the 8515B-50 and 8515B-15 versions, sensitivity is 6±2 mV/psi and 20±6.7 psi, respectively. Combined nonlinearity (hysteresis, nonrepeatability, and nonlinearity) equals 0.5% FSO. Thermal zero shift measures 4% max.

SCC Series strain-gauge transducers from Sensym are designed for cost-sensitive applications where precise accuracy over a wide temperature range is not a critical design consideration. Typical applications include pneumatic controls, automotive diagnostics, medical equipment, and environmental controls. Each member of the series costs $9.90 and features an IC sensor element housed in a single-in-line package. You have a choice of three devices with full-scale pressure

Computer-based techniques facilitate sensor design

Thanks to CAD and micromachining techniques, the latest generation of silicon sensors are sophisticated devices with performance levels far exceeding those found in older-technology chips. Chips with onboard, laser-trimmed calibration and temperature-compensation resistors, for example, are now available in high volume. You can also buy extremely low-pressure sensor chips—less than 1 psi full scale—in large quantities. Today, maximum sensor output nonlinearity is routinely 0.25%.

All these achievements require the most elaborate design, analysis, and manufacturing automation tools and techniques available. Finite element modeling (FEM) programs, for instance, are mechanical-analysis tools that designers can use to predict the operation and performance of complex 3-dimensional shapes such as sensors. Such tools allow designers to calculate and optimize the sensitivity, nonlinearity, resonant frequency, and damping coefficients of new sensor structures before making commitments to expensive tooling.

In addition, FEM programs enable designers to predict the difficult, but important, interactions between the chip and the package. High-performance, high-speed computer workstations, and programs such as ANSYS, make it possible to obtain highly accurate results. By reducing the development time and experimental tooling and materials costs, modeling significantly reduces sensor cost. In effect, a designer can build, test, and optimize a sensor on the computer before any investment in actual hardware takes place.

Circuit-analysis software performs a function similar to that of FEM. According to the application requirements, the computer will integrate the sensor's electrical performance with that of the signal-conditioning circuitry. Designers can, for example, test active correction coefficients and temperature coefficients before actually building a sensor. And, they can use feedback from such computer testing to modify the required chip and circuit specifications to increase performance or decrease cost.

Test, calibration, and trim procedures also have become more sophisticated as the complexity of sensor chips increases. For advanced sensor systems, designers must use computers and modeling to obtain cost-effective solutions for electrical-design, manufacturing, test, calibration, and final-trim specifications.

As users demand sensors with higher accuracy specifications, the need for precision and long-term stability in semiconductor diffused or implanted resistors becomes crucial. Silicon process modeling can predict process variations. These predictions provide input on device specifications and distributions in these specifications before fabrication of the first chips begins. Sensor designers can use these same models to evaluate new processing concepts for improvements in product yield, long-term stability, and device reliability.

After defining and modeling device specifications, designers must convert their engineering concepts into hard tooling. Again, computer-design systems are essential. Computer-graphics terminals can quickly and accurately digitize the various mask levels necessary to fabricate silicon-based sensors. These systems can also rapidly implement design modifications to speed up development schedules.

Computer-aided test systems complete the computer-aided design/analysis process. During the release of early-production-run sensors, computer-aided test systems provide designers with immediate feedback on device performance and correlate this information with design goals. Computer-aided test systems also give engineering and manufacturing groups continuous, on-line, up-to-date, readily available information on yield and on the distribution of crucial specifications for mature sensors already in production.

Acknowledgment

Housed in convenient, low-cost single-in-line packages, Sensym's SCC Series sensors are designed for applications where precise accuracy is not a prime system consideration.

ranges of 5, 15, and 30 psig (pounds per square in. gauge). All units feature internal temperature compensation for operation over 0 to 50°C. Although optimized for this temperature range, SCC sensors do operate from −40 to +125°C. The guaranteed span-temperature error is less than 0.75% FSO, and the combined linearity, hysteresis, and repeatability error is less than 0.5% FSO.

IC Sensors' Models 151 and 154 are solid-state strain-gauge devices that utilize a 316 stainless-steel housing to provide compatibility with most harsh media. The devices are available in gauge-, sealed-gauge-, and absolute-pressure versions that handle full-scale readings of 5 to 300 psi. Static accuracy is ±0.25%, and the operating range spans −10 to +80°C.

Model 154 includes integral laser-trimmed resistors that provide calibration and temperature compensation over the 0 to 50°C range. When the sensor is drawing a 1.5-mA supply current, the nominal output span is 100 mV. For the Model 151, you must provide compensation by using three external resistors (the manufacturer supplies the correct resistance values). Again, for a 1.5-mA supply current, the nominal output span equals 100 mV. The zero-pressure output equals ±1 mV, and the zero and span temperature coefficients correspond to ±1%. The sensors cost $60 (OEM qty); delivery is stock to 60 days ARO.

Motorola's MPX2200 silicon, piezoresistive pressure

Compatible with various liquid and gas media, PT11 sensors from Revere feature a full-scale measurement capability ranging from 100 to 10,000 psi.

sensors each contain, on-chip, a monolithic shear-stress strain gauge, diffused thermisters, and a thin-film resistor network. The pressure sensors are laser trimmed and therefore provide span and offset calibration as well as temperature compensation over −40 to +125°C.

The MPX2200 Series costs $10 in quantities of 50,000 and is available in either basic-element packages for absolute- and differential-pressure measurements or in ported packages for measuring differential, absolute, gauge, gauge-vacuum, gauge-axial, and gauge-axial-vacuum pressure. Over the 0- to 30-psi (0 to 200 kPa) absolute- and differential-pressure ranges, the sensors' 0- to 40-mV analog output is extremely linear. At 25°C, the linearity equals ±0.1% FSO typ and ±0.25% FSO max. The sensitivity is 0.2 mV/kPa, and the typical zero-pressure offset is ±0.05 mV. Temperature effects

on hysteresis, full-scale span, and offset are ±0.5% FS, ±0.5% FS, and ±0.5 mV, respectively.

Micro Switch's 14PC Series are also piezoresistive, strain-gauge types residing on a silicon chip, but these sensors feature four piezoresistors, an integral sensing diaphragm, and are enclosed in miniature, wave-solder-compatible packages. Internally, an elastomer O-ring surrounds the pressure-sensitive diaphragm, leaving it exposed to pressure media applied through the ports, which are ultrasonically welded in place. You can select seal material to fit specific application requirements.

The series is available in both gauge- and differential-measurement versions with full-scale pressure ranges of 5, 10, and 15 psi. Repeatability and hysteresis accuracy translates to ±0.75% FSO. Linearity is 0.5% full scale. The sensors operate from 10V dc supplies and dissipate 20 mW. Their full-scale output, when operating from a 10V dc supply, equals 250 mV. The price is $10.24 (500).

Handling harsh environments

Model 1224 pressure transducers from Foxboro/ICT boast a proprietary 316 stainless-steel/oil-media interface that isolates the solid-state piezoresistive sensing element from excessive shock and vibration. The units' 0- to 100-mV output has a ±0.02% repeatability spec. Available in both gauge-pressure and absolute-pressure versions that cover full-scale pressure ranges from 15 psig/psia to 5000 psig, the sensors cost $135. Standard devices have ±0.5% FSO max static accuracy; ±0.25% is available as an option. Maximum thermal error is ±2% FSO over the −20 to +180°F compensated temperature-operating range. The devices are designed specifically to accommmodate rugged operating conditions and come with a 3-year warranty.

Revere's PT11 pressure sensor finds use as a primary control component in hydraulic systems, air-conditioning systems, engine monitoring, refrigeration units,

compressors, and industrial-control systems. The seven models that make up the line feature full-scale measurement ranges spanning 100 to 10,000 psi. The average combined error for any unit equals ±0.05%.

The 100-psi sensor is constructed of 2024-T351 aluminum; the 250-, 500-, 1000-, 3000-, 5000-, and 10,000-psi devices are constructed of #17-4 PH stainless steel. The minimum burst-pressure limit for all models is greater than 500% of range, and the safe-overrange limit is 200% of full scale. The supply voltage can be 12V ac or dc. The full-scale output is 2 mV/V±20%, and the operating range covers −40 to +150°F. Prices range from $40 to $57, depending on quantity.

The TJE high-precision, wet/wet differential-pressure transducer, available from Sensotec, is engineered for pressure ranges of 50 to 500 psi. The bidirectional device sells for $950, specs 0.1% full-scale accuracy, and

Designed for applications requiring surface-pressure measurements, Endevco's Model 8515B transducer features hybrid temperature-compensation circuitry for stable operation over −54 to +121°C.

Offering full control of variable-speed pump motors, the 150B and 150C transducers from Robinson-Halpern are designed to solve measurement and control problems in sprinkler-system water tanks.

is designed to accommodate fluid or gas media in both ports. Features such as stainless-steel construction and built-in overload protection provide a high degree of durability in harsh industrial environments. The bonded-foil, strain-gauge-type Model TJE employs a 10V dc supply to produce a standard 2-mV/V output; a 4- to 20-mA output is optional. The operating range extends from −65 to +250°F. Zero-offset and span temperature effects are both 0.25%/°F.

Viatran's 22 Series strain-gauge-type transducers are available with either a mV/V output (Model 122,

$479) or 1 to 6V dc output (Model 222, $525). The use of military-grade components makes possible a −60 to +250°F operating range. The units are available in versions with full-scale pressure-measurement capabilities of 50 to 10,000 psig and psia. All feature an accuracy of better than ±0.4% FSO.

The transducers are compensated for an operating range of 70 to 170°F. Temperature effects on span and zero are ±2% max. Model 122 operates from a 10V ac/dc supply voltage, whereas Model 222 operates from either 12 or 28V dc. The full-scale output for the 122

Manufacturers of pressure sensors and transducers

For more information on pressure sensors and tranducers such as those discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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Div of Honeywell
11 W Spring St
Freeport, IL 61032
(815) 235-6600
Circle No 677

varies from 1 to 2 mV/V. Long-term stability equals ±0.25% max for six months, and repeatability is better than ±0.1% FSO. The units will mount in any position and have proof- and burst-pressure specs of 1.5 and 5 times rated pressure, respectively.

The SA devices from Data Instruments are designed to work in applications demanding a rugged, reliable transducer. The units' design isolates the pressure measurand from the electronic hybrid circuitry, allowing the transducers to accommodate media such as oil, gas, saline solutions, blood, hydraulic fluids, alcohol,

freon, ammonia, acids, and gasoline. Full-scale pressure ranges extend from 15 to 50 psia and 100 to 5000 psis (pounds per square in. sealed gauge). Each device is computer-trimmed for calibration and temperature compensation to ensure unit-to-unit interchangeability of ±1%. The transducers' 5V output precludes the need for external amplification. Accuracy (including the effects of nonlinearity, hysteresis, and repeatability) is within ±1% of span. Long-term stability measures ±1% FSO over one year.

The SA transducers function from supply voltages in

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Yellow Springs Instrument Co Inc
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Yellow Springs, OH 45387
(513) 767-7241
Circle No 701

the 9 to 20V dc range. Although the units have a 30 to 185°F compensated operating-temperature range, they will function from −67 to +257°F. Thermal effects on span and zero-offset voltages are ±1%. All units include reverse-polarity and RFI protection as standard features. They cost $209.

Foil-gauge units satisfy low-power needs

Boasting a current consumption of only 1 mA, Trans Metrics' P21L transducers are well-suited to applications where low power consumption is a primary design consideration. In addition, the units provide a 0 to 5V output from 5V dc supplies. They employ foil strain gauges bonded to the nonwetted side of a machined stainless-steel diaphragm-type sensor. There is no contact between the measured fluids and the electrical circuits, so the transducers accommodate any corrosive fluid that does not attack stainless steel.

Relative-, absolute-, compound-, vacuum-, and differential-pressure types are available in full-scale measurement ranges of 15 through 15,000 psi. All models cost $395. The transducers will operate over the −30 to +180°F range and are compensated for operation from 0 to 160°F. Zero-balance and nonrepeatability-error specifications are ±2% FSO and 0.2% FSO, respectively. The static error band (including nonlinearity, hysteresis, and nonrepeatability) measures ±1% FSO for models below 150 psi and ±0.5% FSO for all others.

The signal-conditioning circuitry consists of a low dropout regulator, a voltage doubler, a negative-voltage converter, and an amplifier. Because of the nega-tive-voltage converter, P21L transducers provide an output of 0V at zero pressure, thereby eliminating the need to trim out any voltage offset. The signal-conditioning circuitry also contains field-adjustable zero-balance and span potentiometers. These adjustments are located behind weather-tight plugs.
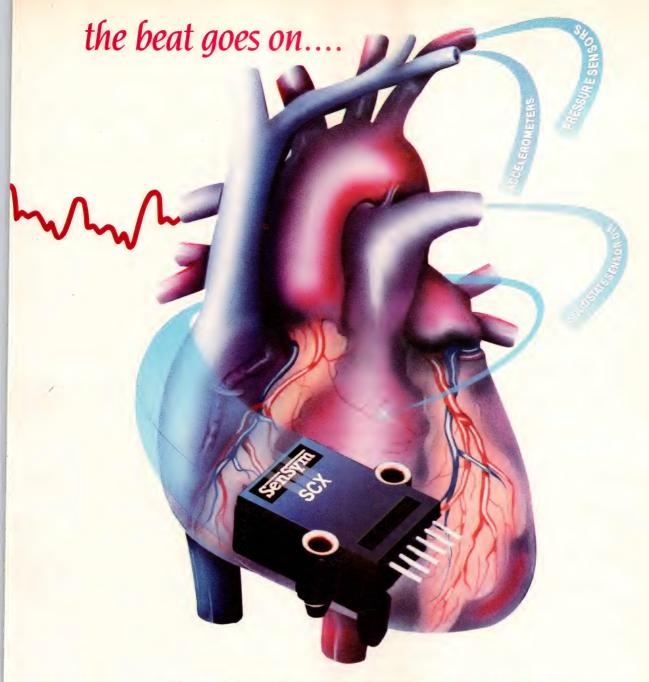
The Model PA194SH from West Coast Research is a micropower transducer ideal for use in salt water, corrosive fluids, and hostile environments. Capable of working in a submerged condition, it operates from approximately 1 mW and provides a full-scale output of 1V or higher. High sensitivity is a key feature of the PA194SH. At 600 ft of water, for example, it is capable of resolving 1 part in 72,000 (0.0014%). Output nonlinearity is less than 0.05%. The unit is available with an output converter or transmitter to yield either BCD, 4- to 20-mA, 0 to 5V, or other control-signal outputs. The submersible version costs $1250; a reduced-sensitivity version (1 part in 24,000) is available for $850.

Medical uses—no problem for foil units

The PPS-1 from Thermometrics costs only $76 and is designed for invasive use in measuring pressure at selected anatomical sites, and, more specifically, for use in thermal-dilution catheters and wedge-pressure catheters. It does accommodate noninvasive applications, too, however. The sensor features a distal tip mount, which attaches to a catheter tube. The silicone rubber diaphragm is at the front face of the sensor, and the

Developed for laboratory and biomedical use, PPS-1 sensors from Thermometrics monitor changes in both pressure and temperature.

Offering wet/wet media compatibility, Micro Switch's 14PC Series is assembled using a TAB (tape automated bonding) process and elastomer O-ring seals.

rear section serves as a shank that attaches to the catheter. Three wires and an atmospheric vent tube extend from the shank.

The sensor measures pressures over the range of −30 to +300 mm of mercury (Hg), and it operates over the range of 15 to 45°C. Overpressure capability extends from −100 to +1200 mm. The sensor operates from 5 to 10V dc supply voltages. Sensitivity at 25°C equals 5 to 10 mV/V/mm Hg. Zero balance is ±75 mm Hg, and the combined linearity and hysteresis error equals ±2 mm Hg. The zero-drift spec (over time and temperature) measures 0.3 mm Hg/°C max and 3 mm Hg/24 hours, respectively.

The number and variety of available strain-gauge transducers attests to their popularity. Nonetheless, other technologies still command a piece of the market. LDVT transducers represent one such technology. Compared with strain-gauge types of sensors, LVDT transducers rely on a transformer coil for the sensing element. Such transducers are unaffected by mechanical strain, making them extremely reliable.

LVDT transducers find an industrial home

Robinson-Halpern's Models 150B and 150C pressure transducers feature a wide zero- and span-adjustment capability that makes them well-suited to solving pressure-measurement and -control problems in auxiliary water tanks such as those used for sprinkler systems. The $325 units can provide precise liquid-level measurement in elevated tanks or water towers even if the instrumentation is located at ground level. Using only a small portion of their pressure-range capability, they maintain full control of variable-speed pump motors. Users can compress the transducers' span from 100 to

Combining varied media compatibility with low cost, Model 151 and 154 sensors from IC Sensors measure full-scale pressures from 5 to 300 psi with ±0.25% accuracy.

15% of the rated range, and suppress the zero-offset voltage by as much as 85%. Zero and span controls are externally accessible.

Models 150B and 150C measure the pressure of liquid or gas media in gauge, differential, or absolute units. They are available in nine versions featuring full-scale capabilities of 1.5 to 300 psi; accuracy is ±0.5% of the user-calibrated range. The devices operate over the −40 to +176°F range, and they are temperature-compensated over the 25 to 150°F range. Their cast-aluminum housing has a NEMA-1 rating. An internal regulator, which features polarity-reversal protection, allows the devices to operate from unregulated power sources.

The P-3061, a member of the P-3000 Series from Schaevitz, has a low-pressure-measurement-range capability. It is available in gauge- and differential-pressure versions capable of measuring 0 to 2 in. of water to 100 psi. The transducer operates from an unregulated 10 to 32V dc supply, consumes only 1.2 mA, and provides a 0 to 5V dc output. The P-3061's total static error is less than ±0.5% of its full-range output (FRO); a ±0.25% FRO spec is available as an option. The operating range extends from −40 to +175°F. The cost is $300.

Kaman Instrumentation Corp also employs inductive technology in its pressure-sensor offerings. The KP-1911 high-temperature pressure-measuring system is an integrated transducer system that operates at temperatures of 1100°F. It includes a pressure sensor/transducer (with 50,000-psi capability), cabling, and signal-conditioning circuitry. The cabling has two sections joined by a transition connector—a metal-sheathed high-temperature section, and a flexible twisted-pair section that connects to the system's electronics.

The sensor can operate in media such as liquid sodium, steam, plastics, and petrochemicals. The system output is an analog voltage directly proportional to the applied static or dynamic pressure. The sensor uses internal impedance variations to measure static and dynamic absolute pressure. Gauge- and differential-pressure-measurement versions are also available. The gauge sensor has a vent that provides an atmospheric reference, and the differential sensor includes a tube that allows you to provide a dry-gas reference pressure.

The KP-1911's housing is alloy 718; the cable sheath is alloy 600. The patented 2-coil sensor design in essence cancels temperature effects and provides a compensated operating range of −100 to +1000°F. Each sys-

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tem has user-adjustable zero and gain controls. Prices start at \$4340.

Although nowhere near as popular or prevalent as strain-gauge or LDVT transducers, piezoelectric transducers still deserve a mention. Advances in crystal technology have made possible piezoelectric transducers that measure high-pressure amplitudes and also produce high outputs at low-pressure levels.
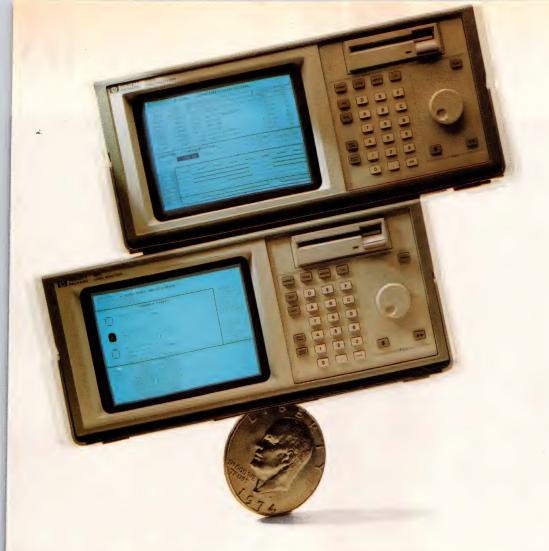
Piezoelectric sensors have clean outputs

The Series 102A from PCB Piezotronics serves as a good example. This line of seven high-frequency pressure tranducers differs in sensitivity, full-scale ranges, and discharge time-constant values. Frequency tailoring minimizes resonant-frequency amplitude when you subject the transducers to extremely fast step-pressure inputs. This tailoring produces a low-impedance (100Ω), high-voltage (5V) nonresonant output signal that can drive long coaxial cable in field, factory, and underwater environments.

The transducers' pressure-measurement capability ranges to 5000 psi. The usable and maximum pressure-rating specs are 10,000 and 15,000 psi, respectively. The sensitivity equals 1 ± 0.05 mV/psi, and the resolution measures 0.1 psi. Series 102A transducers are priced at \$460.

The transducers are almost free of ringing and other internal resonance effects that can distort the signal. Their internal structure employs a compression-mode quartz element with an integral compensating accelerometer to reduce vibration sensitivity and to suppress resonance effects. Matching the resonant frequency, and the acceleration sensitivity of the compensating element, to that of the pressure-sensing element accounts for the nonresonant operation. **EDN**

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CAE software uses algorithms instead of schematics

Drawing logic schematics isn't the only way to create ASIC designs. You can also use algorithms to automatically generate the net list for your hardware design—and you can do so in about one-tenth of the time that it often takes to complete a schematic.

Jay R Southard, *Algorithmic Systems Corp*

Using algorithms to design your hardware can simplify and clarify the design process as well as reduce by as much as 90% the amount of time and money you spend on it. Although engineers customarily associate schematic design with hardware and algorithmic design with software, this need not always be the case. Hardware and software are really just media for implementing your design. Schematics and algorithms, on the other hand, are design methods.

The Ascyn synthesizer transforms your algorithm directly into an ASIC foundry's net list. It also simulates designs, determines clock rates, and automatically generates test vectors. The package, written in LISP, is an artificial-intelligence logic synthesizer that can run on VAXs and personal computers.

Using this synthesizer, you can program your de-sign's algorithm and then either compile it for a simulation run, or synthesize a net list for a specific ASIC foundry's process. After the software generates a net list, the ASIC foundry can tell you how much the circuit will cost to make.

The synthesizer is neither a schematic-capture package nor a silicon compiler. Silicon compilers work by converting high-level schematic specifications into ASIC layouts. The synthesizer, on the other hand, translates algorithms directly into net lists. How the manufacturer lays out the hardware devices is irrelevant to the algorithmic synthesizer's operation.

The algorithmic synthesizer isn't great for every type of design. Designs larger than 10 pages of Ascyn code probably won't fit in 10,000-gate gate arrays, which are generally the largest available. Moreover, any synthe-sized ASIC will of course be faster than the correspond-ing algorithm running on a standard computer, but it's unlikely to be more than 50 times faster at best.

Synthesized designs can be larger and slower than carefully crafted, schematic designs. At the 1000-gate level, the average synthesizer-generated ASIC is about 10% larger than the best schematic implementation of the same function. However, at about 2000 gates and above, the algorithmic synthesizer is better than sche-matic capture at minimizing chip size because a synthe-sizer looks over the entire IC and finds shareable resources.

You can't make a general, quantified comparison of

the speed of an algorithmically designed ASIC with the speed of a schematically designed ASIC. Rather you must evaluate them on a case-by-case basis.

Three key traits characterize synthesizer

The synthesizer's ability to transform algorithms into net lists stems from three key characteristics of the package: its frequent use of master-slave registers, its method of assigning operators to operations, and the way it implements Boolean functions.

Although the master-slave register plays only a minor part in schematic designs, it's fundamental to algorithmic designs. If you write in any computer language:

$$B := B+A$$

what you really mean is:

- Sample the values of variables on the right-hand side of the assignment operator.
- Perform the indicated operation (in this case an addition).
- Hold the resulting value.
- Update the values of the variable on the left-hand side of the assignment operator with the held results.

This sequence defines exactly what a master-slave register does.

The synthesizer's master-slave registers have three inputs: data (word-wide), latch enable (a single-bit signal), and clock. If the latch-enable signal is 0, then the register retains its stored value; if it's 1, then the register gets updated in accordance with the data input, the clock, and the master-slave rules. In **Figs 1, 2,** and **3,** the master-slave registers are boxes with parallel data inputs and a latch-enable single-bit signal. The clock line is implicit.

Operators vs operations

The synthesizer's second key characteristic is its method of assigning operations to operators. For the purposes of this article, operations are the primitive elements of an algorithm. They are the instructions that apply to specific variables at specific times. In contrast, operators are the primitive elements of a schematic. They represent the objects that are eventually connected together to make an integrated circuit. Good logic design involves the art of packing the required operations into the least expensive, highest-performance set of operators.
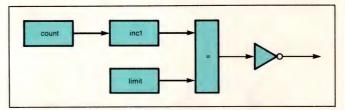
Fig 1—The algorithmic logic synthesizer transforms *a simple limit-checking code fragment into this circuit.*
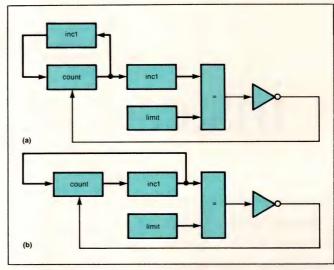
Fig 2—The synthesizer automatically condenses *the redundant operations in* **(a)** *into a single operator in* **(b).**

Using the synthesizer, you can try various design options. You can, for example, write a series of operations either sequentially or in parallel. Thus you can write two lines of operations sequentially:

$$A := A-1 \quad B := B+A$$

or in parallel:

$$\text{(par} \\ A := A-1 \\ B := B+A)$$

The parallel construction includes two operations in a single cycle. The synthesizer can implement the sequential operations with only a single physical operator that can alternately add or subtract (such as an ALU), but not do both at the same time. The parallel version, on the other hand, needs two physical operators to execute both operations simultaneously: It's faster but it requires more hardware.

In some cases, the synthesizer only has to assign a

separate operator to each operation. For instance, consider this small fragment of code in Fortran:

.NOT. (LIMIT .EQ. (COUNT + 1))

The corresponding piece of Ascyn code is:

(not (= limit (inc1 count))

Working under the assumption that these operations must execute in one clock cycle, the synthesizer transforms this algorithm into the circuit in **Fig 1** (the program can generate schematics of this sort at any point in the design cycle). The thick lines in **Fig 1** highlight word-wide data paths; the thin line is an unregistered, single Boolean signal (a "wire" variable in the Ascyn language). For this simple algorithm, every operation has its own operator.

Now consider a slightly larger piece of code:

(if (not (= limit (inc1 count))) (setn-word count
(inc1 count)))

According to the rules of the Ascyn language, the synthesized hardware must execute these operations in one clock cycle. The hardware must therefore perform two "inc1" operations in parallel. **Fig 2a** meets this requirement by including two "inc1" operators, but that solution is very inefficient.

The synthesizer solves the problem by recognizing that both "inc1" operations increment the same variable ("count"); it then synthesizes by applying its fan-out rule and generates the circuit in **Fig 2b**.

To see how the synthesizer would handle a slightly more complicated design, consider the following set of operations that must be sequential (**Program 1**):

(setn-word A (− (+ A B) D)) (setn-bit BOOL
(= LIMIT (− C D)))

If you designed the circuit so that each step is performed separately, you would create the configuration in **Fig 3a.** The synthesizer, however, recognizes that because these operations are sequential and not parallel, they can share operators (**Fig 3b**). This streamlined circuit substitutes a multiplexer and a little more control wiring for a subtractor—a good tradeoff.

Note the control box in **Fig 3a.** Normally, a hardware designer designs everything in the data path except the code for the control section (the data path includes all

the registers and arithmetic operators through which data is processed). Programmers later specify the control code so that the data path executes the higher-level algorithm desired at the time. In contrast, the synthesizer automatically generates all code for the data path, including the control code.

When you want to estimate an ASIC's performance, algorithmic design facilitates identifying the critical path, which is difficult to do from schematics. In the **Fig 3** designs, for example, the critical path depends on the control code. With one control code, the critical path might flow from A and B through the +, MUX, −, and = operators all the way to BOOL. With another control code, the critical path might only flow through the +, MUX, and − operators (**Program 1,** in fact, defines this path). Thus you can easily determine the critical path if you look at the algorithm; but if you just look at the schematic, the critical path is obscure.

To further illustrate this point, consider that a second algorithm exists that generates the same data path as the previous algorithm but not the same control section:

(set n − word A (− C D))
(set n − bit BOOL (=(−(+ A B)D)LIMIT))

It's possible to determine the different critical paths by

(a)

(b)
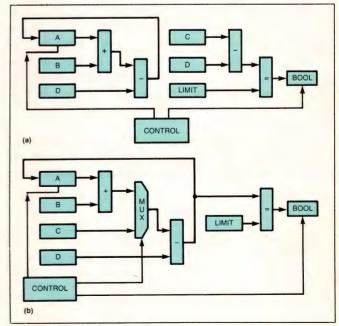
Fig 3—The synthesizer maximizes the use of expensive operators, such as the subtractor in (a) by employing a multiplexer for sequential operations (b).

A synthesized ASIC is not likely to be much more than 50 times faster than the same algorithm running on a standard computer.

analyzing the algorithms, but not if you look at the schematics—which are identical.

The third key element of the Ascyn synthsizer is its Boolean implementation, which differs from the more common Boolean reduction. Most Boolean reductions produce sets of sum-of-products expressions. By DeMorgan's law, these expressions can be realized as 2-level NAND-NAND implementations. But NAND-NAND implementations are not always practical. Consider the high fan-in NAND gate in **Fig 4a**. Such high fan-in gates pose two problems: They are slow, and they're not available in gate arrays. In fact, if you do find an 8-input NAND-gate entry in your foundry's cell library, it's almost certain to be a macro that expands into the primitive cells in **Fig 4b**.

In many cases, the particular high fan-in gate that you need is neither a primitive nor a macro available in a given foundry's library. If you were using normal design methods, you would use the next highest size available and simply tie off some of the inputs. In comparison, if the Ascyn synthesizer can't find exactly the right size in the cell library, it generates from primitives the size needed. To do this, the synthesizer uses a series of rules that transforms and minimizes gates. For example, if an 8-input NAND gate does not exist, the synthesizer generates the circuit in **Fig 4b**.

By analogy, you might expect that the synthesizer would transform a 5-input NAND gate into the set of primitives in **5a**. Instead it goes beyond simple Boolean reduction, and applies DeMorgan's law several more times to generate the circuit in **Fig 5b**. In this way, the synthesizer achieves optimal Boolean implementation. Not only does the design in **Fig 5b** have one less gate than the one in **Fig 5a**, but in some circumstances, it's also faster.

The step-by-step designing of a complex ASIC algorithmically provides a more practical example of how the synthesizer works. Consider a closest-threat
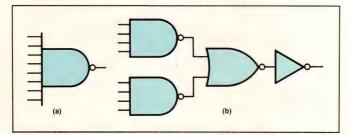
Fig 5—The synthesizer develops the exact-sized gate required. *Although (a) is one possible expansion of a 5-input NAND gate, the synthesizer repeatedly applies DeMorgan's law to achieve an even simpler circuit (b).*

alert subsystem. The system monitors a scanning device (such as a radar or video detector) and then determines and reports the object nearest to a selected set of X,Y coordinates. First, a master processor specifies a set of X,Y coordinates. The ASIC then checks these coordinates against the next frame of data from the scanning device and all subsequent frames until the master selects a new set of coordinates. When the ASIC detects a new closest threat, it alerts the master processor, which then can obtain the current closest object's X,Y location (the alert signal remains high until the next interrogation) (**Fig 6**).

The closest-threat alert subsystem executes algorithms to perform five tasks:
- Input coordinates from the master processor.
- Output coordinates and alarm the master processor.
- Process the pixel data from the scanner.
- Compute the distance from detected objects to the coordinates supplied by the master processor.
- Update the closest threat and alert the master processor if necessary.

Before deciding that an ASIC is the best way to implement the closest-threat subsystem, you must first determine the throughput requirements of the subsystem. The distance calculation seems to be the most critical; the other algorithms seem much less computationally complex. The scanning device scans 256 lines of 256 points each. A frame consists of a framing bit followed by 65,536 data bits. A data bit of 1 indicates that an object exists at the point then being scanned in the frame.

Fig 4—Simple Boolean reducers often produce results that *require high fan-in NAND gates (a). In actuality, such gates in a foundry's cell library are macros that expand to the circuit in (b).*

If X_L and Y_L are the X and Y values of the coordinates selected by the master processor, then the distance from X_L, Y_L to any (X,Y) coordinate is:

$$\sqrt{(X-X_L)^2 + (Y-Y_L)^2}.$$

This simple formula is very computationally intensive however. The following algorithm approximates $\sqrt{a^2+b^2}$ without recourse to squaring or square roots:

$$g = \text{MAXIMUM} \begin{cases} |a| \\ |b| \end{cases}$$

$$l = \text{MINIMUM} \begin{cases} |a| \\ |b| \end{cases}$$

$$c = \frac{7}{8}\, g + \frac{1}{2}\, l$$

$$\text{APPROXIMATE SQUARE ROOT} = \text{MAXIMUM} \begin{cases} c \\ g \end{cases}$$

The subsystem must process 65,536 bits (or pixels) per frame. The number of frames per second depends on the scanning device; the device in this example displays 60 frames per second (a typical number). The subsystem must therefore have a throughput rate of about 4M pixels/sec or better.

Standard μP won't work

You can rule out using a standard μP. The fast magnitude-approximation algorithm needs about 20 instructions. At a clock rate of 16 MHz, and assuming 4 cycles per instruction (both are optimistic estimates), an advanced standard μP can do no better than 0.2M distance computations per second.

You could try other algorithms. For example, you could buffer a frame's worth of data and perform a spiral search. Or, rather than use an approximation, you could note that $(d+1)^2 = d^2+2d+1$, and compute successive values of distance recursively from the beginning of a scan. Using the synthesizer, you can evaluate both the advantages and disadvantages of these two algorithms.

Another hardware option to consider is a programmable logic device (PLD). Unfortunately, the arithmetic required for this application immediately disqualifies

standard PLDs because the carry action of multibit arithmetic implements poorly as a sum-of-products Boolean function.

Yet another possibility is to use a ROM. The distance calculation is completely combinational—it doesn't require saving any data from one input to the next. Because the X and Y inputs are 8 bits each, the resulting distance may be as large as 360, thus requiring 9 bits. This magnitude implies a 64k×9-bit ROM, which is hardly a standard size. Even if you did have such a part, you would still need some auxiliary logic to implement the other, system-oriented, parts of the problem (eg, comparison against current minimum, alerting the master processor).

Code implements distance calculation

The code in **Listing 1** implements only the distance calculations and does not include any I/O functions. The first line names the ASIC as "mag," and declares the default integer word size to be 9 bits wide. The next section, starting with the keyword "def," declares the types of the variables—in this case "input," "output," and "wire" ("wire" variables are unregistered, single-value Boolean variables).

The last section, starting with "always," defines the algorithm. The keyword "always" starts an endless loop that executes everything that follows continuously. The Ascyn language uses a prefix notation, so that (>= x xl) denotes a conditional test that is true if x is greater than or equal to xl, and is false otherwise. Therefore, when the first three program lines following the "always" says:

(if (>= x xl) (set-word dx (− x xl))
(set-word dx (− xl x)))
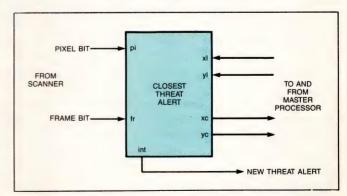
Fig 6—The closest-threat alert subsystem processes a high-speed bit stream from a scanning device and gives a master processor the coodinates of the closest object.

this code fragment means that if x is greater than or equal to xl, then dx is assigned the value x−xl; otherwise, dx is assigned the value xl−x. In other words, this code fragment guarantees that dx is the positive difference between x and xl. (Comments start with a ";" and continue to the end of the line.)

The second program line treats dy similarly. The next program section finds the minimum and maximum of dx and dy. In this case, if dx is greater than or equal to dy, the code does two things in parallel: It assigns the value of dx to g, and it assigns the value of dy to l. The parallel action is exactly the opposite when dy is greater than dx.

The next section creates the approximation c according to the algorithm. The operator >> is a right-shift command and can take several options, including an option for the number of bits to shift. Note that ⅞=1−⅛. Finally, the program selects the maximum of g or c to be the d output.

In order to submit this program to the synthesizer and discover how fast the algorithm will run, you obviously must choose a foundry's cell library. For the closest-threat subsystem, several are available. This

example uses the California Devices Inc (CDI) 2-μm double-level metal-cell library.

To estimate the maximum frequency, the synthesizer analyzes the critical path, taking fan-out capacitive loading into account. This estimate stops short of actually converting the net list into a physical layout and calculating the speed based on the chip's geometry —that's the task of the foundry. The package's simulator estimates that the ASIC's maximum clock frequency will be 4.57 MHz.

Further, this algorithm consumes 742 physical cells of a CDI gate-array chip. The cell count indicates how expensive production is going to be. The average gate-array chip comprises 2,000 of these cells, and the foundry makes up to 10,000-gate chips available (chips with more gates cost more of course).

These manufacturing specifications do not apply to other foundries. To see how large this design will be (and how much it will cost and how fast it will run) using other foundries' gate arrays or standard cells, you must resynthesize the algorithm using their libraries.

In this case the CDI chip is an acceptable size. If it weren't but you only needed a 10% improvement, you

LISTING 1—BASIC DISTANCE-CALCULATION ALGORITHM

```
(system mag 9
    (def
        (x input word *) (xl input word *) (dx wire word *)
        (y input word *) (yl input word *) (dy wire word *)
        (g wire word *) (l wire word *)
        (c wire word *) (d output word *)
        )


    (always
; dx = absolute value of (x - xl)
        (if ()= x xl) (set-word dx (- x xl)) (set-word dx (- xl x)))
; dy = absolute value of (y - yl)
        (if ()= y yl) (set-word dy (- y yl)) (set-word dy (- yl y)))
; g and l are max and min of absolute values
        (if ()= dx dy)
            (par (set-word g dx) (set-word l dy))
            (par (set-word g dy) (set-word l dx)))
; c = 7/8 g + 1/2 l
            (set-word c (+ ()) l).            ; 1/2 l +
            (- g ()> g bit-0 3))))            ; 7/8 g
; approximate square root = max of g , c
            (if ()= c g) (set-word d c) (set-word d g))
            ))
```

might try altering the fan-out ratio. However a 10% change often isn't sufficient, and you must consider more radical measures.

Pipelining shortens critical paths

One possible measure is pipelining. It gives you a larger design but a shorter critical path. Yet pipelining also changes the chip's operation because the outputs are delayed some number of cycles behind their associated inputs. The rest of the system must be able to accommodate this latency.

You have the option of pipelining the distance calculation. This sort of pipelining is very easy to effect. Just designate some of the variables to be "saved" variables rather than as unregistered ("wire") variables. Selecting variables l and g is a good choice because they are roughly in the middle of the algorithm (**Listing 2**). Thus pipelining here yields the greatest improvement in performance for the least cost. The first pipeline stage calculates l and g from dx and dy. The second stage uses l and g to calculate c and d. Except for the declarations of the type of variables, the code is unchanged from **Listing 1**.

Selecting the same foundry's library as before, and resynthesizing, yields a chip that runs at 7.72 MHz instead of 4.57 MHz. However, the chip now consumes 842 physical cells instead of 742. So far, this result is exactly as you would expect: You've traded time for space. You could make more pipeline stages. For example, dx and dy could be pipeline registers—so could c. Each time you add a pipeline stage, you should improve the throughput at the expense of increased chip area.

One of the primary advantages of an ASIC over standard parts is that you can achieve exactly the right I/O configuration as well as exactly the right computation on a system-by-system basis. Depending on the processor bus to which you are connecting, the data bus could, for example, be bidirectional. If you are using one of the Intel processors, you might find that the address and data buses were multiplexed. A standard chip that does not meet the processor's interface requirements requires extra chips for the interface. On the other hand, you can change the I/O algorithm to accommodate such processor-bus variations.

The processor needs to be able to load the ASIC with new values of xl and yl (**Listing 3**). In specifying I/O, for example, you can assign some of the processor's

LISTING 2—DISTANCE ALGORITHM WITH PIPELINING

```
(system mag 9
    (def
        (x input word *) (xl input word *) (dx wire word *)
        (y input word *) (yl input word *) (dy  wire word *)
        (g saved word *) (l saved word *)    ;pipeline registers
        (c wire word *) (d output word *)
        )
    (always
; dx = absolute value of (x - xl
        (if ()= x xl) (set-word dx (- x xl)) (set-word dx (- xl x)))
; dy  = absolute value of (y - yl)
        (if ()= y yl) (set-word dy  (- y yl)) (set-word dy  (- yl y)))
; g and l are max and min of absolute values
        (if ()= dx dy )
            (par (setn-word g dx) (setn-word l dy ))
            (par (setn-word g dy ) (setn-word l dx)))
; c = 7/8 g + 1/2 l
        (set-word c (+ ()> l)           ; 1/2 l +
        (- g ()> g bit-0 3))))          ; 7/8 g
; approximate square root = max of g , c
        (if ()= c g) (set-word d c) (set-word d g))
        ))
```

LISTING 3—MEMORY-MAPPED I/O TO CUSTOMIZE ASIC FOR A μP

```
;The processor expects to receive an interrupt when the closest threat changes.

(system com 9
  (def
     (ad-hi input word 8 0 *)      ; The inputs are only
     (ad-lo input word 8 0 *)      ; 8 bits wide,
     (do input word 8 0 *)         ; When used in a 9-bit operations, msb will be 0
     (di tri-state word *)
    ; di will be hi-impedence unless explicitly set during a clock cycle
     (rd input bit *)
     (wr input bit *)
     (xc saved word *)
     (yc saved word *)
     (dc saved word *)             ; saved value of current distance
     (intfl saved bit *)           ; generate an interrupt if the newly calculated
     (int output bit *)            ;    distance chages from the old value of dc
     (xl saved word *)
     (yl saved word *)
     (y saved word *)
     (x saved word *)
     (fr input bit *)
     (pi input bit *)
     (restart saved bit *))        ; hold until next
  (always
     (set-bit int intfl)           ; int is always the same as interrupt flag
     (if wr
         (if (reduce and ad-hi)                ; ad-hi all ones
             (par (set-bit restart bit-1)      ;     resync calculation
                  (if (bit-lsb ad-lo)
                      (setn-word yl do)         ;     odd -> set new yl
                      (setn-word xl do)))))     ;     even -> set new xl
     (if rd
         (if (reduce and ad-hi)                ; ad-hi all ones
             (par (setn-bit intfl bit-0)       ;     clear pending interrupt
                  (if (bit-lsb ad-lo)
                      (set-word di yc)          ;     odd  -> send current yc
                      (set-word di xc)))))      ;     even -> send current xc
;********
;  now input frame sync and manage x and y counters,
     (if fr
         (par (setn-word x 0) (setn-word y 0)
              (if restart
                  (par (setn-bit restart bit-0)  ; clear pending restart
                       (setn-word dc 511))))      ;  and set dc to max.
     (if (bit-msb y) ()            ; too many rows - wait for frame sync
     (if (bit-msb x)
         (par (setn-word x 0) (setn-word>
```
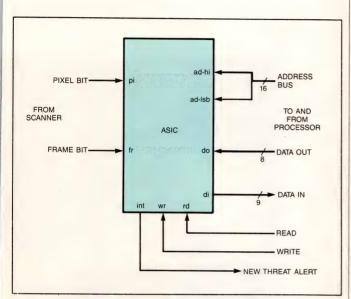
*Fig 7—**Adding data and address buses** to the ASIC customizes it for a particular μP.*

memory-address locations to the ASIC. If the processor writes to an even address in the $FFXX_{HEX}$ block, it loads a new xl value, and similarly loads a new yl value if the address is odd.

If the processor reads an even address in the $FFXX_{HEX}$ block, the chip will output the closest threat's x coordinate for the duration of the read signal. If the address is odd, the chip outputs the yl coordinate, and the processor generates the "Read" and "Write" signals, which the chip then inputs.

The chip maintains the x and y values; these values are derived from the framing bit ("fr") that comes from the scanning device. **Fig 7** reflects these modifications in the initial closest-threat-alert diagram. When synthesized, the completed chip uses 1342 gates and operates at 4 MHz. **EDN**

Author's biography

Jay R Southard is the president of Algorithmic Systems Corp (Braintree, MA). Previously he worked for MetaLogic, MIT's Lincoln Lab, Draper Labs, and General Instruments. Jay received a BA from Grinnel College and an MSEE from Stanford. He belongs to the IEEE.

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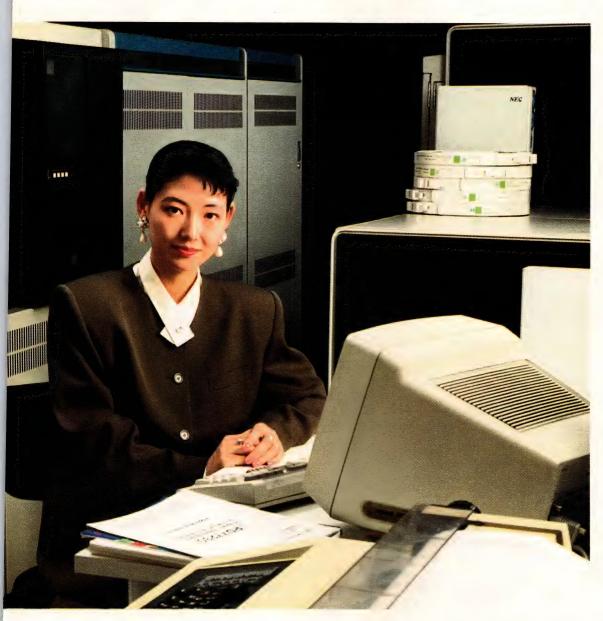
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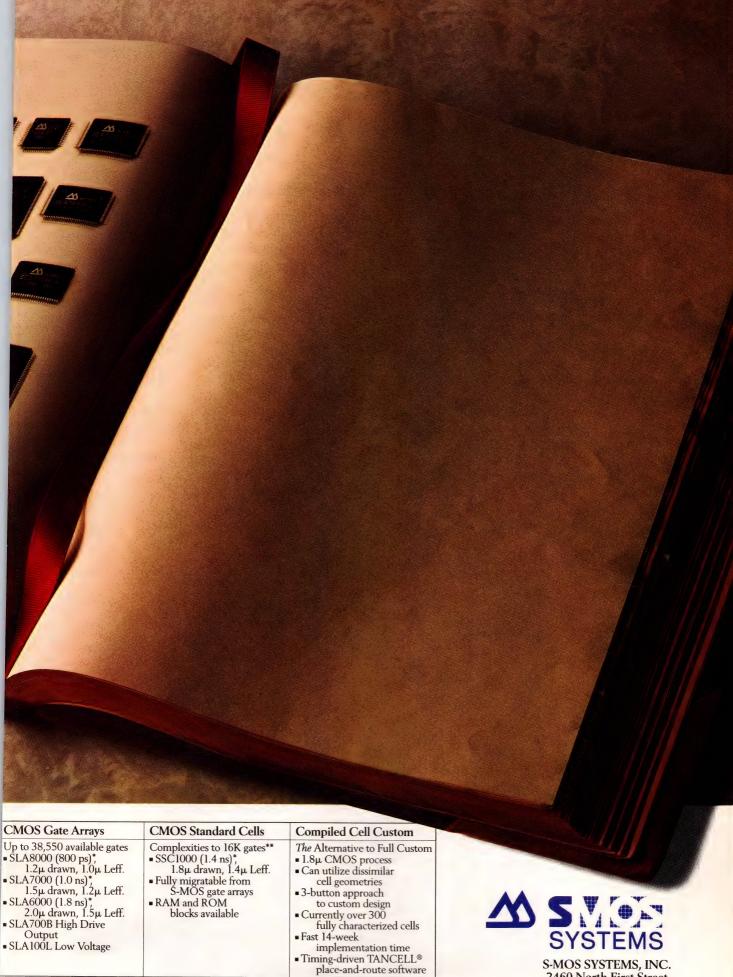
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The Enhanced Performance Architecture (EPA), a subset of the MAP specification, allows networks to provide fast, noise-immune communication over short distances. By applying a single VLSI chip that implements most of the EPA functions in silicon, you can speed your network's response time without a huge software-development effort.

Rhonda Alexis Dirvin and Anne-Marie Larkin
Motorola Inc

If you're building or extending a factory network that includes intelligence, programmable controllers, and systems that must respond quickly to their controlling computer, you'll find the Manufacturing Automation Protocol (MAP) too slow for your purposes. To let machines or sensors send status information and command acknowledgment to their controlling computer quickly, you can implement the Enhanced Performance Architecture (EPA), a streamlined version of the MAP specification that takes into account the networking requirements of the workstations, PCs, and intelligent machines in a factory environment—requirements that are vastly different from those of large computers.
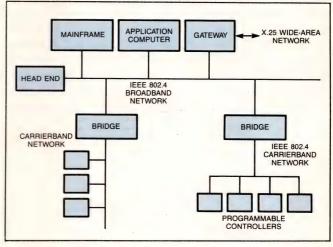
Fig 1—A broadband network connects the major nodes of a MAP system, which uses all seven layers of the ISO/OSI model. Local carrierband networks connect the smaller computers to sensors and intelligent machines that require high performance and short response times.

The EPA, created by the SP-72 committee of the Instrument Society of America (ISA) and the MAP Enhanced Performance Architecture Task Group, accommodates a wide variety of machines by dividing the total network into a hierarchy of subnetworks, each of which could meet a different set of performance requirements (Fig 1). The Process Industries Special Interest Group also played an important part in pressing for and helping to define the EPA.

The initial MAP specification concentrated on creating a backbone network in the factory to provide

The Enhanced Performance Architecture provides a high-performance, low-cost link between process-control stations and a MAP network.

communication among the large computers at the administrative level. This type of communication did not need to be especially fast; several seconds might elapse between file transfers, for instance. On the lower level of the factory, however, machines such as numerical controllers and robots need to perform information transfers at much shorter intervals (tenths of milliseconds, in some cases). At present, it's not possible to obtain this high performance if all communications must pass through the full seven layers of the OSI protocol, which the MAP uses. Further, it takes significant memory and horsepower to run all seven layers. If your task is merely to provide a network for the low-cost machines at the factory's lower level, you probably won't be able to justify the expense of all that memory and horsepower.

The EPA solves that problem by specifying only layers 1 and 2, an interface, and layer 7. The remaining layers (3 through 6) perform functions that are not needed in the low-level nodes served by the EPA. The interface between layer 2 and layer 7 puts the data into a format compatible with the Manufacturing Message Specification (MMS). Reducing the number of layers of ISO/OSI software not only yields an improvement in network performance (because EPA nodes execute fewer instructions to perform a given function), but also
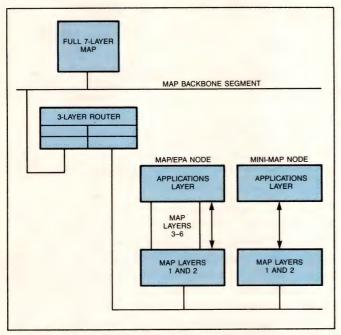
reduces software-design costs, because the system designer has fewer layers to deal with.

For one thing, the specifying bodies chose broadband technology as the physical layer for the backbone of the MAP, because it can operate over long distances (miles) and because it has high noise immunity. EPA subnetworks, on the other hand, operate only over distances of 500 to 1000 ft; they could therefore use either carrierband or baseband technology in the physical layer. Both of these technologies are far less expensive than broadband technology.

Today's broadband modems cost from $700 to $1500 and require a head-end remodulator (one per network), which sells for around $10,000. Carrierband modems cost from $400 to $600 and require no head-end remodulator. This price comparison does not take into consideration the fact that carrierband technology will soon be available in silicon form—a fact that will drop the carrierband price to approximately $100 per node. Carrierband technology also lets you save on space, because you'll probably need only one board instead of two to accommodate the hardware. The primary reason to choose carrierband over broadband, therefore, is economic.

When considering alternatives to broadband technology, the specifying bodies preferred carrierband over baseband for several reasons, including cost: Carrierband is somewhat less expensive than baseband. More important, however, is that carrierband has much better noise immunity, because it frequency-modulates a constant-amplitude carrier signal instead of amplitude-modulating a constant-frequency signal, as the baseband technique does. Its higher noise immunity makes carrierband more suitable for use in an electrically noisy factory environment.

EPA subnetworks contain a variety of node types

The Enhanced Performance Architecture embraces several different types of stations that fulfill different purposes; the types include Mini-MAP, MAP/EPA, and router nodes (**Fig 2**). Mini-MAP nodes can communicate only with each other and with MAP/EPA nodes over the subnetwork, using the 3-layer EPA architecture. Direct communications of this type are easy and efficient. The MAP/EPA node is also a carrierband device, but it contains facilities for converting data from 3-layer format to 7-layer format and vice versa.

All the communications between a Mini-MAP node and a backbone node take place via a MAP/EPA node and a router. The MAP/EPA node performs all of the

Fig 2—Mini-MAP nodes serve small machines and programmable controllers. They communicate with backbone nodes via MAP/EPA nodes and a router.

conversions between the 3-layer EPA architecture and the 7-layer MAP architecture. The router is a 3-layer device that can segment data frames to ensure that they conform to the maximum size limitations, both on the backbone side and on the EPA-segment side. It also contains both broadband hardware that connects to the backbone network, and carrierband hardware that connects to the EPA segment (subnetwork). Routers' frame-segmenting capability is the reason that the specifying bodies preferred routers over bridges or gateways as the links between the backbone and EPA segments. Bridges are too simple and can only filter addresses; gateways, which perform full protocol conversion, are more complex and more expensive than is necessary for the MAP/EPA link.

Redundancy maintains network integrity

A subnetwork may contain multiple MAP/EPA nodes, both to provide redundancy and to improve performance. If one of the MAP/EPA nodes fails, another one can perform the same functions; it thus prevents the subnetwork from being isolated from the backbone. If you expect to have a substantial amount of network traffic between the subnetwork and the MAP backbone, you should consider providing more than one MAP/EPA node in order to maintain acceptable levels of performance. Indeed, the MAP specification requires that a subnetwork contain at least two MAP/EPA nodes before it can be classified as an EPA segment.

EPA functions allow very simple nodes

One function that was not in the original MAP specification but was added to the EPA is the IEEE 802.2 Logical Link Control (LLC) type 3 Acknowledged Connectionless Service. This function allows EPA station A to ask station B a simple question, such as "What is your temperature?" While station A still holds the token, station B can respond immediately with a simple answer (for example, "58°C"). This function can achieve response times of around 5 μsec, because station B doesn't have to obtain the token and then establish a new communication link.

By using the LLC type 3 feature, you can greatly reduce the cost of attaching simple devices to an EPA segment of the network. Temperature and pressure sensors, for example, do not need to participate in the token-passing ring; they only have to be able to respond properly when they're sent an LLC type 3 request

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ISO/OSI model specifies seven layers

The MAP specification is based on the International Standards Organization's Open Systems Interconnect (ISO/OSI) model primarily because the ISO/OSI model already has widespread international support. Now the US federal government, too, has chosen the ISO/OSI model for the new networking procurements described in the Government Open Systems Interconnection Profile (GOSIP) document.

The ISO/OSI model breaks the communications task into seven sections, or layers. Each layer has a duty to perform or a service that it must provide to the layer immediately above it. ISO specifies what services must be provided, but it doesn't specify the manner of implementing them. **Table A** shows the name and function of each layer of the ISO/OSI model. Immediately above layer 7 are any user application programs, which are not part of the ISO/OSI model.

TABLE A—THE SEVEN LAYERS OF THE ISO/OSI MODEL

NAME	FUNCTION
LAYER 7—APPLICATION	PROVIDES ALL SERVICES THAT ARE DIRECTLY COMPREHENSIBLE TO APPLICATION PROGRAMS
LAYER 6—PRESENTATION	TRANSFORMS DATA TO AND FROM NEGOTIATED STANDARDIZED FORMATS
LAYER 5—SESSION	SYNCHRONIZES AND MANAGES DIALOGUES
LAYER 4—TRANSPORT	PROVIDES TRANSPARENT RELIABLE DATA TRANSFER FROM END NODE TO END NODE
LAYER 3—NETWORK	PERFORMS MESSAGE ROUTING FOR DATA TRANSFER BETWEEN NODES
LAYER 2—DATA LINK	MANAGES ORDERED ACCESS TO THE MEDIUM AND DETECTS ERRORS INVOLVED IN THIS PROCESS
LAYER 1—PHYSICAL	ELECTRICALLY ENCODES AND PHYSICALLY TRANSFERS DATA OVER THE MEDIUM

EPA networks use carrierband technology as the medium because it's less expensive than broadband and has better noise immunity than baseband.

TABLE 1—LLC TYPE 3 PRIMITIVES PROVIDED BY THE MC68824

ACKNOWLEDGED CONNECTIONLESS DATA-UNIT TRANSMISSION SERVICE

PRIMITIVE	DESCRIPTION
L__DATA__ACK.request	USED TO SEND A DATA UNIT WITH ACKNOWLEDGMENT TO ANOTHER NODE
L__DATA__ACK.indication	USED TO INDICATE THE RECEPTION OF A NON-NULL, NONDUPLICATE LSDU FROM A REMOTE DATA-LINK NODE
L__DATA__ACK__STATUS.indication	USED TO INDICATE WHETHER THE PREVIOUS LSDU TRANSMISSION REQUEST WAS SUCCESSFUL

ACKNOWLEDGED CONNECTIONLESS DATA-UNIT EXCHANGE SERVICE

PRIMITIVE	DESCRIPTION
L__REPLY.request	USED TO REQUEST AN ACKNOWLEDGED CONNECTIONLESS DATA-UNIT EXCHANGE
L__REPLY.indication	USED TO INDICATE RECEPTION OF AN RWR FRAME
L__REPLY__STATUS.indication	USED TO CONFIRM RWR FRAMES

REPLY DATA-UNIT PREPARATION

PRIMITIVE	DESCRIPTION
L__REPLY__UPDATE.request	USED TO INDICATE THE NEED TO UPDATE A RESPONSE
L__REPLY__UPDATE__STATUS.indication	USED TO CONFIRM THAT A RESPONSE WAS UPDATED

frame. Very simple hardware can provide them with this ability; the node can consist merely of an enhanced token-bus-controller chip, a carrierband chip, some memory to hold the response, and some mechanism for updating the memory as required.

VLSI chip embodies the EPA functions

To meet the requirements for low cost and high performance that are driving the development of the EPA, you can apply a device such as the MC68824 token-bus controller (TBC), which implements the EPA functions in silicon. Motorola recently enhanced the chip so that it now implements both the Media Access Control (MAC) portion of the IEEE 802.4 standard and the Receiver portion of the IEEE 802.2 LLC type 3 Acknowledged Connectionless Service (**Table 1** summarizes the latter).

These services provide a means, at the data-link level, of sending a message from one node to another and of receiving an acknowledgment message without establishing a separate data-link connection. This feature yields the very fast response time that the applications require. In addition, the MC68824 provides two separate methods of bridging: hierarchical and IBM-defined source routing. The chip allows the user to choose between powerful address mechanisms that permit group-address recognition and multidrop operation.

Some of the MC68824's enhancements include a reduced-data-structure mode for increased performance, a FIFO option for increased reliability, and a bus-analyzer mode that lets you run the TBC as a powerful protocol analyzer. The chip can now perform serial data transfers over the network at speeds ranging from 10k to 12.5M bps, and it can accommodate system clock rates from 10 to 16.67 MHz.

The MC68824 functions as an intelligent peripheral device to a host microprocessor. The TBC is a full MC68000 bus master; it has on-chip DMA facilities for managing tables and frame buffers located in shared memory, and these DMA facilities transfer data frames to and from a shared memory with minimal intervention from the host μP. A fully linked buffer-management scheme allows the queueing of frames during transmission and reception. You can configure the TBC bus interface to handle both 8-bit and 16-bit
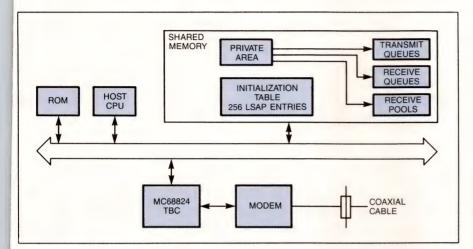
Fig 3—An EPA node consists of an enhanced TBC, a host CPU, memory shared by the host and the TBC, and a modem. The node can be very simple, because it needs to implement only the lower three layers of the ISO/OSI model.

data transfers in either Motorola/DEC or Intel/IBM data formats. **Fig 3** shows the MC68824 in a typical intelligent system environment.

EPA is one of chip's three operational modes

The MC68824 has three main operational modes: the TBC mode, the EPA mode, and the bus-analyzer mode. In the TBC mode, which is the default mode, the MC68824 provides a full MAC implementation as well as support for LLC types 1 and 3. Running the TBC in its default mode allows the host μP to perform the LLC functions (or equivalent functions) in software.

In the EPA mode, the MC68824 performs the receiver functions of the Acknowledged Connectionless Service of the LLC sublayer, as well as operating normally when it receives a nonrequest-with-response frame. The receiver portion of LLC type 3 is the most time-critical, and it performs much better when implemented on chip.

To use the EPA mode, the host must set a bit in the initialization table, and must also add an LSAP (Link Service Access Point) table to the end of the initialization table. This table has an entry for each of the 128 possible individual LSAPs and one for each of the 128 group LSAPs. Each LSAP entry contains user information as well as LSAP status information (such as whether or not the LSAP is active). For each active LSAP, the host prepares a response and puts the pointer to the response in the corresponding entry of the LSAP table. The host also updates the response when necessary.

When a receiving station running in EPA mode finds a Request with Response (RWR) encoded in the frame control of an incoming frame, the station looks at the corresponding LSAP entry in the LSAP table. If the

RWR frame requests data, the receiving station will return the data that the LSAP entry points to, provided that the LSAP is active. If the LSAP is not active, the station returns a NACK. If the RWR frame does not request data, the station merely returns an ACK (if it has received the frame correctly) or a NACK (if it has received the frame incorrectly).

In the bus-analyzer mode, the MC68824 is not part of the logical ring, but it receives all frames. This feature makes the TBC an ideal chip for use in a protocol-analyzer application. In this mode, the TBC time-stamps all frames, so it can measure the elapsed time between network events.

Host, TBC communicate through shared memory

The TBC also makes use of a simpler data structure. The MC68824 and the host communicate with each other through shared memory. This shared memory comprises two tables and some buffer structures that store received frames or frames awaiting transmission. The two tables are called the initialization table and the private area.

The initialization table contains the initial parameters that the host loads into the private area by giving the Initialize command at power-up or after a reset. The table also holds the command-parameter area, the interrupt status words, some statistics, and, if the TBC is running in the EPA mode, an LSAP table.

The command-parameter area has two main uses: The host employs it mainly to pass parameters to the TBC in conjunction with a command, and the TBC uses it to return parameters to the host in response to a command. The TBC continuously updates two Interrupt Status Words (ISWs) to indicate status changes. Flags in the ISW, filtered by an interrupt status mask,

determine whether or not a particular event will generate an interrupt. ISW1 keeps track of events that relate to the local system. For example, one of the flags in ISW1 informs the host that the TBC has received a data frame. ISW2 keeps track of events that relate to the network. One of the flags in ISW2, for example, informs the host that the TBC has detected a duplicate MAC address on the network.

The statistics area of the initialization table holds network statistics, such as "number of who_follows events." The host may collect all the statistics or may disable the collection of two items (Tokens_passed and Number_of_tokens_heard). Also, the TBC keeps track of various types of modem errors in the statistics area.

The private area contains mainly MAC operational parameters and statistics; therefore, the TBC uses it primarily as an extra storage area. Hi_Priority_Token_Hold Timer, for example, is a MAC operational timer that you can specify in the private area if you use the priority option. IEEE 802.4 specifies this and many other timers. Among the MAC statistics kept in the private area is the Last Token_Rotation_Time, which is the observed time measured from token arrival to token arrival.

The private area also holds the pointers to the various buffer structures used for receiving and transmitting data frames. After power-up or reset, the host initializes the private area by storing the appropriate values in the initialization table and then issuing the Initialize command. After initialization, the host can view or modify the private area by issuing the appropriate commands. However, in order to avoid conflicts, the host must not directly access the private area while the TBC is participating in a network.

Linked buffers hold frame queues

The TBC uses linked buffer structures (**Fig 4**) to provide four transmit queues and four receive queues in accordance with the IEEE 802.4 message-priority scheme. The fully linked buffer structures consist of frame descriptors, buffer descriptors, and data buffers. Each frame descriptor contains control information pertaining to a frame sent or received, plus links to the next frame descriptor and to the buffer descriptor. The buffer descriptor contains the data buffer's attributes, such as the user-specified offset, which points directly to the data in the data buffer. This feature is useful for appending upper-layer protocol headers without moving the data. Each buffer descriptor also contains links to the next buffer descriptor (if there is one) and to the data buffer. Finally, the data buffers contain the actual data.

This linking scheme makes it easy for the host's software to build data frames: The scheme lets each
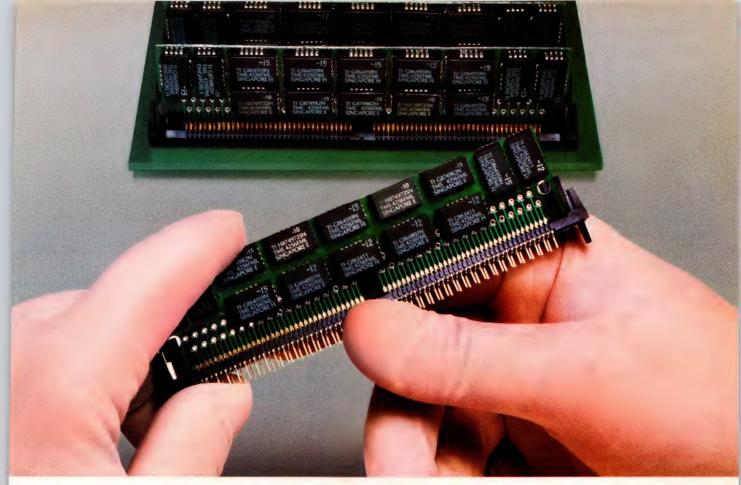
MAP uses IEEE 802.4 token-bus protocol

At the physical and data-link layers, the MAP uses the token-passing bus protocol specified by IEEE standard 802.4. The protocol was chosen because it's deterministic; that is, the maximum allowable time for any station to access the medium is known. A token bus is also very flexible, because its topology allows you to add stations to or delete them from the network without disrupting network operations. The token-bus protocol also clearly defines error-related functions such as recovery from lost or multiple tokens, token-passing failures, inoperative transmitters or receivers, and duplicate station addresses.

A token is a specific bit sequence in the frame-control portion of the frame. When a station holds the token, it has the right to transmit. When that station has finished transmitting all of its frames, or when the timer that tracks the station's maximum token-holding time (which is specified by the user) has timed out, the station passes the token to the station having the next lower address. This process continues until the station with the lowest address passes the token back to the station with the highest address.

The station that holds the token periodically polls stations that are connected to the bus (but are not currently part of the logical ring) to see if any station wishes to join the logical ring. If a new station does wish to join the ring, the sending station patches the new station into the ring as its logical successor. For example, if the sending station, A, receives a valid reply from station E, station A patches station E into the ring by making E (instead of B) the logical successor to A.

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software layer append the header information to the data by simply changing a pointer or offset. The MC68824 can also run in a reduced-data-structure mode that combines the frame descriptor, buffer descriptor, and data buffer as one structure.

The reduced-data-structure mode is well suited for receiving frames in systems that require very high throughput rates, because it requires fewer linking operations than the full data structure does, and, therefore, it's faster. In some applications, the higher performance that you get from the reduced data structure is more advantageous than the power and flexibility of the full data structure.

The TBC has a flexible command set

The host processor commands the TBC to perform various functions by writing the appropriate command to the TBC command register. Initialization commands configure the TBC for operation after a hardware or software reset. These commands include Reset, Offline, Load Initialization Table Function Code, Initialize, and Idle. Idle causes the TBC to join the ring.

Mode commands set or clear various modes of TBC operation; the Set/Clear In_Ring_Desired command is typical of this category. Three commands pertain to the transmission of data frames: Start, Stop, and Restart. Parameter commands allow the host to modify or read TBC parameters such as function codes, the pad-timer-preset register, and some of the parameters that reside in the private area.

Test commands allow the host to run diagnostics while the TBC is in the off-line state; these commands test the host/TBC interface, the transmitter, the receiver, and the serial sections of the TBC, as well as the internal sections of the TBC.

Finally, two commands allow the TBC to provide management services to the physical layer of the node. The TBC's serial interface conforms to the IEEE 802.4 Standard Serial Interface. The Standard Serial Interface specifies a set of 10 I/O signals, which are used for data transfer when the TBC is in the MAC mode, and for passing station-management information when the TBC is in the station-management mode.

EPA is gaining acceptance

The Enhanced Performance Architecture fulfills a requirement of the factory floor that the MAP did not previously address: the ability to provide sensors and intelligent machines with a low-cost, high-performance link to the MAP network. However, the fast response times that the EPA requires were initially very difficult to achieve. The EPA is only now starting to gain acceptance because of the emergence of devices such as the MC68824 Enhanced TBC.   **EDN**

Fig 4—The shared memory holds frame descriptors (FDs), buffer descriptors (BDs), and data buffers. The private area holds operational parameters and pointers to the first FD of each message to be queued.

Authors' biographies

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CIRCLE NO 87

Static-system design exploits low-power CMOS

Static CMOS architectures let you customize a design for optimum performance and minimum power dissipation. Capitalizing on the characteristics of CMOS means addressing clock-frequency control before starting the initial design process.

Walter J Niewierski, *Harris Semiconductor*

As every engineer knows, CMOS μPs combine low power with high performance: A CMOS μP's power dissipation is directly related to its frequency of operation. Reducing the operating frequency from 16 MHz, say, to 1 MHz, allows the power-supply current to drop proportionately. An NMOS or bipolar μP's supply current, on the other hand, remains the same regardless of how you manipulate a system's throughput-rate spec.

An NMOS system can be bulky

The benefits of CMOS vs NMOS are readily apparent when you compare datasheet operating specifications. An NMOS 80286 μP, for example, has a typical power-dissipation spec of 3W (I_{IC}=600 mA at 5.25V). In contrast, a CMOS 80C286 μP, when running at a clock rate of 16 MHz, has a maximum operating current of 260 mA.

Operating power also has a ripple effect through a system design. Usually you have to add NMOS memory and NMOS or bipolar peripherals to support an NMOS device. Depending on the size of your system, power requirements may be 25 to 30W, and you may well have to specify a larger and heavier 50W power supply to accommodate future expansion.

You also have to account for the fact that temperatures within an NMOS system can rise significantly. It's not unusual for the temperature of an NMOS or bipolar die to rise 40 to 60°C during operation, and fans and heat sinks are necessary to compensate for this increase. Oftentimes, the system also requires an air filter for the fan. Obviously, you have to design an enclosure large enough to hold all of this equipment—fans, bulky power supplies, and heat sinks.

Because CMOS devices dissipate less power, you can specify smaller power supplies. Lower power dissipation also means that the system will run at a lower ambient temperature. Heat sinks and fans are unnecessary, and vents can be shut to ensure a clean operating environment. Sealed enclosures can also be smaller and lighter.

For these reasons, many NMOS- and bipolar-device architectures are now available in CMOS. Furthermore, CMOS technology is amenable to static-circuit design, and NMOS is not. Static circuits allow you to customize your design to balance speed requirements and power considerations.

Static ICs run on any clock frequency from dc to the maximum circuit operating specification. In a dynamic circuit, if the clock frequency falls below a manufacturer-specified minimum, the circuit can lose or alter data,

Static circuits run on any frequency from dc to the maximum circuit operating specification.

and thus the memory cells require refreshing at a certain rate to maintain valid data. You can put a static μP in a standby mode simply by stopping the clock signals, and even if you stop the external clock indefinitely, the device will retain data. When you reinitiate the CPU clock signal, the system starts up where it left off.

The ability to stop the clock also allows you to perform single-step operations during system development. This valuable method of debugging allows you to inspect the system bus and other functions for proper operation by manually stepping through the clock cycles. Single-stepping—and therefore the elimination of real-time data transfers—can simplify debugging significantly.

By taking advantage of opportunities to manipulate the system clock during your initial design, you can mix and match standby, low-frequency, and high-frequency

operations to achieve the most performance for the least power. You can design a μP system that allows the software executive routine to power down the entire system or just portions of the system not in use (certain I/O sections, for example, or file-maintenance areas).

A clock controller eases design

To ease the implementation of static-operating modes in CMOS systems, clock controllers are available for various μPs. **Fig 1** illustrates a CMOS system configuration using a Harris 82C85 static clock controller to interface directly to the maximum-mode status lines ($\overline{S}_2$, $\overline{S}_1$, and $\overline{S}_0$) of either a Harris 80C86 or 80C88 μP. The three control lines ($\overline{S}_2/\text{Stop}$, $\overline{S}_1$, and $\overline{S}_0$) on the 82C85 let you control the operation of the system clock with 80C86/80C88 software. Essentially, the μP controls the clock by issuing a Halt instruction in software.

The status lines of the 80C86/80C88 identify the type

S_2	S_1	S_0	CHARACTERISTICS
0 (LOW)	0	0	INTERRUPT ACKNOWLEDGE
0	0	1	READ I/O PORT
0	1	0	WRITE I/O PORT
0	1	1	HALT
1 (HIGH)	0	0	CODE ACCESS
1	0	1	READ MEMORY
1	1	0	WRITE MEMORY
1	1	1	PASSIVE
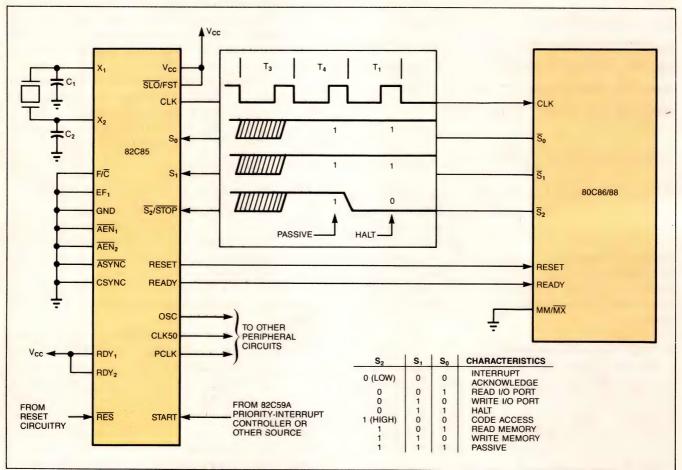
Fig 1—The 82C85 clock controller interfaces directly to an 80C86 or 80C88 CPU operating in the maximum mode. When the controller detects a Halt instruction, it stops the clock.
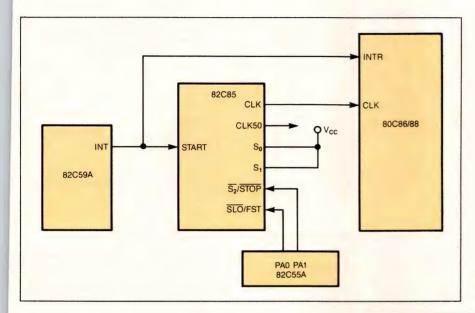
Fig 2—A CMOS peripheral such as the 82C55 can control a clock controller's stop, start, and slow or fast operations.

of bus cycle that the CPU is starting to execute, and are accessible only during maximum-mode operation. Typically, a bus controller uses these status lines to decode the current bus-cycle status of the CPU. **Fig 1**'s truth table shows the status lines for different bus transactions. When operating in the maximum mode, the CPU places the $\overline{S}_2$, $\overline{S}_1$, and $\overline{S}_0$ lines in a 111 state followed by a 011 state to indicate a Halt instruction. The control lines on the 82C85 automatically decode this state sequence to halt the system clock.

You can use a peripheral such as a programmable interface (in this case, the 82C55A) to stop the clock by using the $\overline{S}_2$/Stop line as a stand-alone Stop command **(Fig 2)**. You must tie the $\overline{S}_0$ and $\overline{S}_1$ pins of the 82C85 to V_{CC} to emulate a logic 111 state before applying a logic 0 to the $\overline{S}_2$/Stop line to stop the clock. To place the 82C85 clock controller in a stop-oscillator mode, you tie the F/$\overline{C}$ line low. In this mode, the 82C85 stops the clock synchronously whenever it detects a Halt instruction. Regardless of whether the controller is operating in the fast or slow mode, it will decode a Halt instruction. **Table 1** compares the four operating modes of the 82C85.

Stop the clock!

The 82C85 also offers another way of stopping the system clock. The start-input line on the 82C85 provides independent clock control. A level-triggered active-high input overrides any stop condition. You can control the start-input line, for example, by using an 82C59A priority-interrupt controller **(Fig 2)**. The INT

TABLE 1—COMPARISON OF 82C85's OPERATING MODES

OPERATING MODE	DESCRIPTION	POWER LEVEL	PERFORMANCE
STOP-OSCILLATOR	ALL SYSTEM CLOCKS AND MAIN CLOCK OSCILLATOR ARE STOPPED.	MAXIMUM SAVINGS	SLOWEST RESPONSE DUE TO OSCILLATOR-RESTART TIME
STOP-CLOCK	SYSTEM CPU AND PERIPHERAL CLOCKS ARE STOPPED, BUT MAIN CLOCK OSCILLATOR CONTINUES TO RUN AT RATED FREQUENCY.	REDUCED SYSTEM POWER	FAST RESTART; NO OSCILLATOR-RESTART TIME
SLOW	SYSTEM CPU CLOCKS ARE SLOWED WHILE PERIPHERAL CLOCK AND MAIN CLOCK OSCILLATOR RUN AT RATED FREQUENCY.	POWER DISSIPATION SLIGHTLY HIGHER THAN STOP-CLOCK MODE	CONTINUOUS OPERATION AT LOW FREQUENCY
FAST	ALL CLOCKS AND OSCILLATORS RUN AT RATED FREQUENCY.	HIGHEST POWER	FASTEST RESPONSE

output pin of the 82C59A connects directly to the start-input pin of the 82C85 and the INTR pin of the 80C86/80C88 μP. An external event (such as a key depression) can produce an 82C59A interrupt request, which causes the 82C85 to start the system clock.

If your system must operate continuously but power

During the initial design of a static CMOS system, the designer should anticipate circumstances in which the system can be stopped or run more slowly.

consumption is a concern, you can utilize the slow mode on the clock controller to divide the clock outputs by 256. The 82C85 has a $\overline{SLO}$/FST pin that determines the speed of the system clock. When you apply a logic 1 to the $\overline{SLO}$/FST pin, the frequency of the CLK and CLK50 outputs equals the crystal frequency divided by 3. A logic 0 on the $\overline{SLO}$/FST pin makes the frequency of the CLK and CLK50 outputs equal to the crystal frequency divided by 256.

If you are converting an NMOS or bipolar system to CMOS technology, each device you replace achieves a power savings. **Table 2** shows typical power-supply currents for devices in an 80C88-based system with an 82C85 static clock controller. When the CPU operates at 5 MHz (that is, with a 15-MHz crystal frequency), the total system draws 72 mA (less than 400 mW). The slow mode (20-kHz CPU frequency) reduces the power-supply current by a factor of 3 (24 mA). This mode maintains continuous operation yet gives you the option to switch the system to full speed at any time.

The two stop modes offer the alternative of fast clock turn-on or minimum power dissipation. In the stop-clock mode, the main system oscillator continues to run and permits full-speed operation to resume within three CPU clock cycles (600 nsec at 5 MHz) after the fast mode is reinitiated. The main crystal oscillator
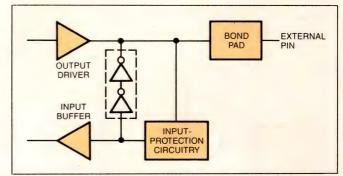
Fig 3—An on-chip bus-hold circuit maintains a valid CMOS logic level on its external pin when a driving source goes to a high-impedance state.

continues to run at 15 MHz (for a 5-MHz system).

The stop-oscillator mode stops the system clock and the main crystal oscillator. The standby supply current for the system referred to in **Table 2** is 752.7 µA, which is less than 4 mW at 5V. When you restart the crystal oscillator, the frequency and amplitude can vary significantly. After the amplitude reaches a specified amplitude, the 82C85 counts 8192 oscillator cycles to ensure crystal stabilization. The stabilization time guarantees that the clock outputs turn on within the specification limits and with the proper phase relationship.

The choice of operating modes depends upon system

TABLE 2—SYSTEM CURRENT DRAIN WITH AN 82C85 CLOCK CONTROLLER

TYPICAL-SYSTEM DEVICES	MODES			
	STOP-OSCILLATOR	STOP-CLOCK	SLOW	FAST
82C85	24.4 µA	14.1 mA	16.9 mA	24.7 mA
80C88	106.6 µA	106.6 µA	173.0 µA	23.8 mA
82C82	1.0 µA	1.0 µA	6.5 µA	1.7 mA
82C86	1.0 µA	1.0 µA	14.0 µA	1.4 mA
82C88	3.8 µA	3.8 µA	14.3 µA	3.5 mA
82C52	1.0 µA	1.0 µA	72.0 µA	151.2 µA
82C54	1.0 µA	3.5 µA	915.0 µA	943.0 µA
82C55A	1.0 µA	1.0 µA	1.2 µA	3.2 µA
82C59A	509.0 µA	509.0 µA	520.0 µA	580.0 µA
HD-6406	4.97 mA	4.97 mA	5.09 mA	5.12 mA
74HCXX PLUS OTHER ICs	90.0 µA	90.0 µA	110.0 µA	2.9 mA
HM-6516	1.9 µA	1.9 µA	132.0 µA	820.0 µA
HM-6616	12.0 µA	12.0 µA	52.5 µA	6.3 mA
TOTAL WITH 6406	5.72 mA	19.8 mA	24.0 mA	71.9 mA
TOTAL WITHOUT 6406	752.7 µA	—	—	—
CPU FREQUENCY	dc	dc	20 kHz	5 MHz
CRYSTAL FREQUENCY	dc	15 MHz	15 MHz	15 MHz

Clock control is the key to designing a minimum-power system.
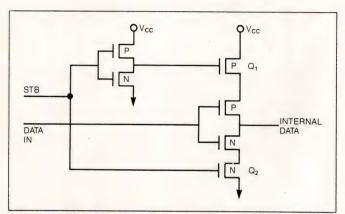
Fig 4—In CMOS devices with gated inputs, *a low logic level on the STB line turns the Q₁ and Q₂ FETs off so that a transition on the data-input line doesn't draw power-supply current.*

priorities. The stop-clock mode delivers the fastest response and return from standby operation, but does so at the expense of higher power dissipation than the stop-oscillator mode. The stop-oscillator mode minimizes power dissipation, but has a longer response time.

Although clock control is key to low-power performance in a static CMOS system, there are other factors of which you should be aware. For example, when the input-voltage level on a CMOS device approaches the minimum V_{IH} (high-level voltage) or maximum V_{IL} (low-level voltage), the p- and n-channel FETs can partially turn on. This condition produces a low-resistance path between V_{CC} and GND and results in excessive power-supply current. Therefore, you must tie all CMOS inputs to V_{CC} or GND in some manner when they are not in use.

Pull-up/down resistors are the most common method of ensuring CMOS input-voltage-level specifications. The resistors maintain valid CMOS voltage levels when a driving source is in a floating high-impedance state. This technique, however, suffers from some disadvantages. First, extra resistors are necessary, which increases both board real estate and cost. Second, the circuit's power dissipation increases because the driving source must supply extra current to the resistors. Needless to say, if you can avoid using pull-up/down resistors, you can improve overall system performance.

Fig 3 shows the bus-hold circuitry that the 80C86, 80C88, 82C55A, and 80C286 devices include to eliminate the need for pull-up/down resistors. When no driving source is present or when a driving source is in a floating high-impedance state, the on-chip circuitry maintains a valid CMOS logic level on specific inputs.

The circuit will maintain this valid CMOS level until an external source overdrives the affected input. The external device must source or sink approximately 400 μA to overdrive the input. Because the bus-hold circuits are active, their current requirements are similar to the leakage currents for an active device: The circuit typically draws less than 10 μA when it isn't switching. This current is in contrast to the current drawn through a 10k-Ω pull-up resistor: 500 μA when the logic level is low.

Excessive current drain can also result when the input circuitry of a CMOS device responds to voltage transitions unrelated to its operation. A typical system has bus transceivers and latches attached to the system bus. The input circuitry of these devices undergoes many signal transitions unrelated to the functional operation of the devices themselves. These unrelated voltage transitions switch the input circuitry of a CMOS device, causing an increase in power dissipation. In addition, if the system bus experiences a high-impedance state (a floating condition), it could result in an indeterminate logic state internal to an attached CMOS device.
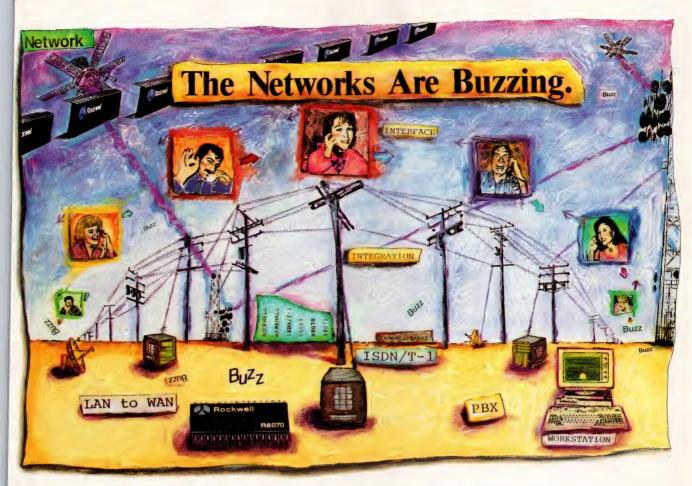
You can eliminate excessive current drain due to unrelated input transitions by using bus transceivers and latches with gated inputs. The Harris Series 82C8X bus transceivers and latches (such as the 82C82/83/86/87) let you gate their data inputs when not in use (**Fig 4**). When the strobe line (STB) is in a active-low state, the upper p-channel FET (Q_1) and the lower n-channel FET (Q_2) turn off. This action removes V_{CC} from the input circuitry so that no supply current flows to GND during unrelated input transitions and the circuit doesn't respond to floating inputs. **EDN**

Author's biography

Walter J Niewierski is a marketing manager at Harris's Semiconductor Product Div in Melbourne, FL. He previously worked for Ford Motor Co and Burroughs Corp before joining Harris eight years ago. Walt has a BSEE from the University of Michigan and enjoys coaching little-league baseball in his spare time.

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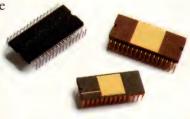
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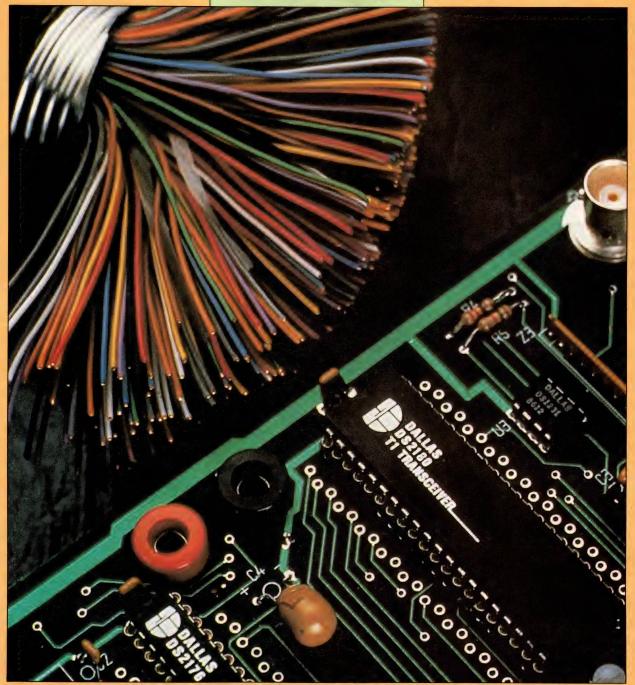
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A

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Advertiser Product Database—May-October 1987. *Staff; EDN NEWS, 12/87, pg 36, 1.5 pgs.*

Selective growth and new DRAM cells share the IEDM spotlight. *Cole, Bernard C, Managing Editor; Electronics, 11/26/87, pg 109, 2 pgs.*

Amplifiers

Cut noise in isolated circuits with variable-carrier amplifier. *Burt, Rod, Burr-Brown; Electronic Design, 04/14/88, pg 101, 3.5 pgs.*

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Simple techniques help you conquer op-amp instability. *Siegel, Barry L, Elantec; EDN, 03/31/88, pg 181, 8 pgs.*

Transimpedance amps: fast yet accurate. *Palmer, Wyn, Analog Devices; Electronics, 01/07/88, pg 151, 4 pgs.*

Use of transimpedance amplifiers minimizes design tradeoffs. *Hansford, Alan, Analog Devices; EDN, 11/26/87, pg 205, 7.5 pgs.*

Analog switches

Eliminate the guesswork in analog-switch error analysis. *Moore, Stephen, Siliconix; EDN, 11/26/87, pg 219, 7 pgs.*

Arithmetic chips/circuits

Building-block chips are busy widening DSP horizons. *Leonard, Milt, Senior Editor; Electronic Design, 03/31/88, pg 68, 7.5 pgs.*

Floating-point milestone: Single-chip processors. *Lineback, J Robert, Managing Editor; Electronics, 03/17/88, pg 77, 1 pg.*

Newest floating-point processors blur architectural distinctions. *Wilson, Ron, Senior Editor; Computer Design, 04/15/88, pg 32, 6 pgs.*

Artificial intelligence

Digital signal processing and AI inherent in consumer electronics. *Staff; Electronic Design, 01/07/88, pg 144, 2 pgs.*

Audio

Analog filtering: top gun for audio. *Ambrose, John, Exar; ESD, 01/88, pg 97, 3.5 pgs.*

Automatic test equipment/techniques

Design for testability creates better products at lower cost—Decade 90 Part 3. *Leibson, Steven H, Regional Editor; EDN, 03/31/88, pg 135, 8.5 pgs.*

Military ATE: capability up, tester inventory down. *Novellino, John, Associate Editor; Electronic Design, 01/21/88, pg 68, 8 pgs.*

Pioneering engineers begin to adopt board-level automatic test generation. *Strassberg, Dan, Associate Editor; EDN, 03/17/88, pg 57, 7.67 pgs.*

B

Batteries

Focus on rechargeable batteries: Economic portable power. *Grossman, Morris, Senior Editor; Electronic Design, 03/03/88, pg 118, 6.5 pgs.*

Board-level computers

Big RISC boxes bust out all over. *Vaughan, Jack, Managing Editor; ESD, 04/88, pg 24, 1 pg.*

Board vendors turn to systems approach. *Wilson, Dave, Editor; ESD, 04/88, pg 17, 2 pgs.*

DSP card fits IBM PC. *Bridges, Jim, Communications Automation & Control; EDN NEWS, 03/88, pg 1, 1 pg.*

Fax-board makers carve out niches. *Harbert, Tammi, Senior Editor/ News; EDN NEWS, 04/88, pg 12, 1 pg.*

Interface turns Mac II into GPIB controller. *DeSantis, Tom, IOtech; EDN NEWS, 04/88, pg 29, 1 pg.*

Low-cost, rugged commercial computers fit military needs. *Conner, Margery S, Regional Editor; EDN, 12/24/87, pg 151, 7.5 pgs.*

Plug-in boards let your personal computer perform parallel-processing tasks. *Mosley, J D, Regional Editor; EDN, 02/04/88, pg 89, 5 pgs.*

STE Bus vies for share of US STD Bus domain. *Harold, Peter, European Editor; EDN NEWS, 04/88, pg 1, 1 pg.*

C

CMOS logic

AC/ACT logic supplies the glue for bus interface. *Funk, Richard E, GE Solid State; Electronic Design, 04/14/88, pg 121, 5 pgs.*

CMOS VLSI sets the direction for new ICs. *Wilson, Ron, Senior Editor; Computer Design, 12/87, pg 79, 9 pgs.*

Chip sets for PC/AT compatibles support faster µPs and shrink board size. *Conner, Margery S, Regional Editor; EDN, 11/12/87, pg 79, 4 pgs.*

Controversy, user doubts continue to embroil advanced CMOS logic. *Wilson, Ron, Senior Editor; Computer Design, 03/01/88, pg 24, 2 pgs.*

Managing power makes CMOS logic systems shine. *Curtis, Rick, Texas Instruments; Electronic Products, 03/15/88, pg 30, 6 pgs.*

Understand CMOS flash ADCs to apply them effectively. *Demler, Michael J, Datel; EDN, 01/21/88, pg 127, 6.5 pgs.*

CMOS technology

Is BiCMOS the next technology driver. *Cole, Bernard C, Managing Editor; Electronics, 02/04/88, pg 55, 3 pgs.*

Jedec simplifies selection of BiMOS, CMOS gate arrays. *LaBuda, Virgil P, Motorola; Electronic Design, 03/17/88, pg 107, 8 pgs.*

Overcome testing hurdles posed by new CMOS logic. *Pino, Dave, Hall, William, National Semiconductor; Electronic Design, 01/21/88, pg 109, 4 pgs.*

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Cache memory

Cache controllers flare memory bottleneck. *Bursky, Dave, Executive Editor; Leonard, Milt, Senior Editor; Electronic Design, 03/31/88, pg 25, 5 pgs.*

Cache tag RAMs hasten main memory response. *Leonard, Milt, Senior Editor; Electronic Design, 03/03/88, pg 19, 3.5 pgs.*

Capacitors

Capacitors chip in for surface-mounting and switching supplies. *Biancomano, Vincent, Technology Editor; Electronic Design, 03/88, pg 25, 5 pgs.*

Special Report: A big cast of SMD passives hits center stage. *Shereff, Jesse, Contributing Editor; Electronics, 02/04/88, pg 103, 6 pgs.*

Clock circuits

Interface a real-time clock chip to the IBM PC or Apple II. *Khan, Adnan, GE Solid State; Alexander, Mark, GE/Intersil; EDN, 11/12/87, pg 209, 7 pgs.*

Communications ICs

Boost fast modem throughput by analyzing dial-up lines. *Berger, Bill, Rockwell International; Electronic Design, 11/12/87, pg 113, 3.5 pgs.*

Data-compression chip eases document-processing design. *Silver, David, Kofax Image Product; Williamson, James, Advanced Micro Devices; Computer Design, 11/15/87, pg 101, 3 pgs.*

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Interface the ISDN to your PC with a voice/data board. *Gulick, Dale, Crowe, Charlie, Advanced Micro Devices; Electronic Design, 12/10/87, pg 85, 4 pgs.*

LAN chip makers grapple in a turbulent market. *Cole, Bernard C, Managing Editor; Electronics, 04/14/88, pg 87, 3 pgs.*

MAPcon takes on factory network configuration. *Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 04/14/88, pg 95, 2 pgs.*

Mainframe network chips ease big interfacing blues. *Cormier, Denny, Senior Technical Editor; ESD, 01/88, pg 17, 2 pgs.*

Mimic's next challenge: Slashing production costs. *Naegele, Tobias, Military/Aerospace Editor; Electronics, 11/26/87, pg 121, 3 pgs.*

New choice in crossbar switching: the IC. *Lineback, J R, Managing Editor; Electronics, 01/21/88, pg 32, 1 pg.*

Processor and communication ICs. *Mokhoff, Nicolas, Senior Editor; Electronic Design, 02/18/88, pg 83, 8.5 pgs.*

Software changes smart modem to smart scope. *Alunkal, John, Codex; Holley, Paul, Holley; Electronic Design, 12/10/87, pg 99, 4.5 pgs.*

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Telecomm ICs offer improved functions for telephone- and PABX-system designs. *Pryce, Dave, Associate Editor; EDN, 01/07/88, pg 55, 5.33 pgs.*

Comparators

Analog comparators achieve high speeds, but application challenges remain. *Shear, David, Regional Editor; EDN, 01/07/88, pg 75, 5.5 pgs.*

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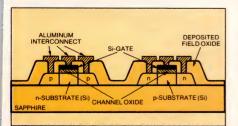
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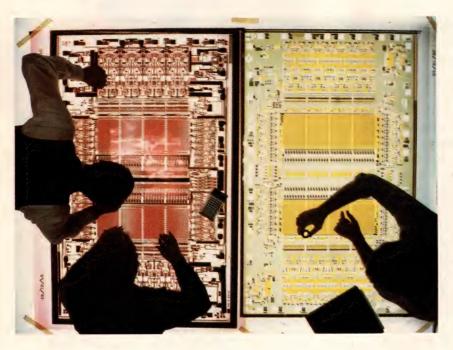
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Computer applications

RISC systems to lead the way in computation-intensive design jobs. *Staff; Electronic Design, 01/07/88, pg 78, 2 pgs.*

When are MFLOPS really MFLOPS. *Aseo, Joseph, West Coast Technical Editor; ESD, 03/88, pg 38, 5 pgs.*

Computer firmware

Chip sets for PC/AT compatibles support faster µPs and shrink board size. *Conner, Margery S, Regional Editor; EDN, 11/12/87, pg 79, 4 pgs.*

Computer languages/compilers/interpreters

Bare Machine Ada solves real-time problems. *Seymour, Burch, Gould; Computer Design, 03/01/88, pg 58, 5 pgs.*

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C interpreters and incremental compilers function as interactive development tools. *Terry, Chris, Associate Editor; EDN, 01/21/88, pg 57, 3.33 pgs.*

Coding languages to change little as libraries offer reusable code. *Staff; Electronic Design, 01/07/88, pg 96, 1 pg.*

Combine forth with other tools for rapid software development. *Payne, W H, Sandia Laboratories; Electronic Design, 01/21/88, pg 103, 4 pgs.*

Digital signal processing: Chips are here, but software isn't. *McLeod, Jonah, Managing Editor; Electronics, 03/31/88, pg 57, 3 pgs.*

Languages coupled with fast processors for high throughput. *Aseo, Joseph, West Coast Technical Editor; ESD, 02/88, pg 26, 1 pg.*

Novel architecture backs high-level languages. *Case, Brian, Olson, Tim, Advanced Micro Devices; Electronic Products, 02/15/88, pg 35, 5 pgs.*

Object-oriented languages reorient programming techniques. *Wilson, Ron, Senior Editor; Computer Design, 11/01/87, pg 52, 6 pgs.*

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Computer operating systems/system software

CAE/CAD suppliers catch some sun. *Collett, Ronald E, Senior Technical Editor; ESD, 03/88, pg 30, 1 pg.*

Developers target Unix and Ada with real-time kernels. *Falk, Howard, Contributing Editor; Computer Design, 04/01/88, pg 55, 11.5 pgs.*

First tron microprocessor gets Japan into the 32-bit fray. *Lineback, J R, Managing Editor; Electronics, 01/21/88, pg 31, 1 pg.*

Instruction-set architecture prepares systems for 1990s. *Bursky, Dave, Executive Editor; Electronic Design, 02/04/88, pg 33, 5.5 pgs.*

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Real-time operating systems. *Small, Charles H, Associate Editor; EDN, 01/07/88, pg 115, 17.5 pgs.*

Satisfactory operating systems for workstations remain elusive. *Staff; Electronic Design, 01/07/88, pg 98, 1 pg.*

Sleight of hand makes MS-DOS multitasking. *Aseo, Joseph, West Coast Technical Editor; ESD, 12/87, pg 47, 3 pgs.*

Software opens door to MS-DOS applications for non-PCs. *Falk, Howard, Contributing Editor; Computer Design, 01/15/88, pg 22, 2.5 pgs.*

Supercomputer software: The floodgates are opening. *Young, Jeremy, Managing Editor; Electronics, 03/03/88, pg 75, 3 pgs.*

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Until OS/2 comes along. *Clarke, Robert M, Contributing Writer; ESD, 04/88, pg 77, 3 pgs.*

Update: 80386 operating systems. *Myrvaagnes, Rodney, Associate Editor; Electronic Products, 02/01/88, pg 18, 1.5 pgs.*

When are MFLOPS really MFLOPS. *Aseo, Joseph, West Coast Technical Editor; ESD, 03/88, pg 38, 5 pgs.*

Windowlike user interfaces link systems and applications. *Williams, Tom, Western Managing Editor; Computer Design, 04/01/88, pg 34, 6 pgs.*

Computer software, application generator

Automatic programming could boost productivity threefold. *Staff; Electronic Design, 01/07/88, pg 94, 1 pg.*

Computer software, communications/networking

Networking software. *Wright, Maury, Regional Editor; EDN, 03/03/88, pg 103, 7 pgs.*

Computer software, design applications

Advanced tools finally start to automate software design. *Schindler, Max, Software Editor; Electronic Design, 11/27/87, pg 61, 7.5 pgs.*

Autorouters debut in PC-based CAE arena. *Harbert, Tammi, Senior Editor/News; EDN NEWS, 01/88, pg 8, 3 pgs.*

CASE tools. *Terry, Chris, Associate Editor; EDN, 04/28/88, pg 111, 7.5 pgs.*

CASE tools emerge to handle real-time systems. *Falk, Howard, Contributing Editor; Computer Design, 01/01/88, pg 53, 14 pgs.*

CASE tools square off to analyze a real-time system. *Schindler, Max, Software Editor; Electronic Design, 04/28/88, pg 103, 10 pgs.*

Evaluate model types before simulating logic circuits. *Moffat, Kent, Carter, Don, Mentor Graphics; EDN, 03/17/88, pg 187, 5.5 pgs.*

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Software lets you design first, pick PLD later. *Warrington, Gene, Minc; EDN NEWS, 03/88, pg 10, 1 pg.*

Software will level the road for parallel processing. *Staff; Electronic Design, 01/07/88, pg 100, 1 pg.*

Spice extensions dynamically model thermal properties. *Filseth, Eric, Analog Design Tools; Jachowski, Mike, Precision Monolithics; EDN, 04/14/88, pg 169, 10 pgs.*

Timing reports: real-time CASE systems emerge. *Aseo, Joseph, West Coast Technical Editor; ESD, 01/88, pg 20, 1 pg.*

Computer software, graphics

AI beefs up gray-scale correlation. *Silver, William M, Schatz, David, Cognex; ESD, 03/88, pg 89, 3 pgs.*

Computer-supported graphics ease software specifications. *Schindler, Max, Software Editor; Electronic Design, 03/03/88, pg 87, 9 pgs.*

Estimating kernels from amplitude spectra. *Krukar, Richard, University of New Mexico; ESD, 12/87, pg 35, 2 pgs.*

Image restoration techniques. *Wilson, Scott R, University of New Mexico; ESD, 12/87, pg 39, 3 pgs.*

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Windowlike user interfaces link systems and applications. *Williams, Tom, Western Managing Editor; Computer Design, 04/01/88, pg 34, 6 pgs.*

Computer software, other

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Computer software, performance measurement

Digital signal-synthesis tools model real-world environments. *Kafadar, Karen, Hewlett-Packard; EDN, 11/12/87, pg 239, 7.5 pgs.*

Computer software, production test

Pioneering engineers begin to adopt board-level automatic test generation. *Strassberg, Dan, Associate Editor; EDN, 03/17/88, pg 57, 7.67 pgs.*

Computer software, program development

Customer training and reverse engineering promise to escalate the acceptance of CASE. *Terry, Chris, Associate Editor; EDN, 03/17/88, pg 73, 4 pgs.*

Program-generation tools for PCs ease IEEE-488 system integration. *Harold, Peter, European Editor; EDN, 04/14/88, pg 71, 6.33 pgs.*

Computer subsystems/peripherals, other

A new look at analyzing peripheral performance. *Hospodor, Andy, I/O XEL; Computer Design, 03/15/88, pg 94, 4 pgs.*

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Input technologies extend the scope of user involvement. *Williams, Tom, Western Managing Editor; Computer Design, 03/01/88, pg 41, 9.5 pgs.*

Computer systems/system design, other

For cost/performance, partition RISC system on bus parameters. *Cates,*

Ron, VLSI Technology; Electronic Design, 11/12/87, pg 121, 6 pgs.

RISC systems to lead the way in computation-intensive design jobs. Staff; Electronic Design, 01/07/88, pg 78, 2 pgs.

Computer-aided design/engineering (CAD/CAE)

ASIC verification: Chasing a moving target. McLeod, Jonah, Managing Editor; Electronics, 11/26/87, pg 79, 3 pgs.

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Design tools advance to keep pace with system complexity. Goering, Richard, Senior Editor; Computer Design, 12/87, pg 103, 8 pgs.

Developing CAE tools target top-down design of complex systems—Decade 90 Part 2. Leibson, Steven H, Regional Editor; EDN, 03/17/88, pg 131, 7 pgs.

EDIF translators begin to open up CAE/CAD systems. Goering, Richard, Senior Editor; Computer Design, 12/87, pg 30, 1.5 pgs.

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Laying out mixed chips takes IBM days, not weeks. Naegele, Tobias, Military/Aerospace Editor; Electronics, 02/18/88, pg 76, 1 pg.

Logic simulation on personal computers: Friend or foe. Milne, Bob, Senior Editor; Electronic Design, 03/03/88, pg 50, 9 pgs.

Modeling strategies simplify board-level simulation. Goering, Richard, Senior Editor; Computer Design, 03/01/88, pg 29, 4.5 pgs.

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Silicon compilers still struggling toward widespread acceptance. Andrews, Warren, Contributing Editor; Computer Design, 02/15/88, pg 37, 6 pgs.

Simulate analog circuit boards without Spice's shortcomings. Walsh, Kevin, Electrical Engineering Software; Electronic Design, 02/04/88, pg 75, 4 pgs.

Simulation accelerators address throughput issues. Goering, Richard, Senior Editor; Computer Design, 03/15/88, pg 42, 5 pgs.

Simulation puts zip into circuit board design. Spadaro, Joseph J, Associate Editor; Electronic Products, 04/01/88, pg 34, 8 pgs.

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Solutions begin to surface for linking board design and test. DeSena, Art, ADS Associates; Computer Design, 03/01/88, pg 34, 5 pgs.

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Spice extensions dynamically model thermal properties. Filseth, Eric, Analog Design Tools; Jachowski, Mike, Precision Monolithics; EDN, 04/14/88, pg 169, 10 pgs.

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Worst-case timing analysis ensures board reliability. Rizzatti, Lauro, Wasilewski, Mary, Teradyne; Computer Design, 11/15/87, pg 90, 6 pgs.

Computer-aided manufacturing/testing (CAM/CAT)

Solutions begin to surface for linking board design and test. DeSena, Art, ADS Associates; Computer Design, 03/01/88, pg 34, 5 pgs.

Conferences/conventions/shows

A torrent of future products at the solid state conference. Cole, Bernard C, Managing Editor; Electronics, 02/18/88, pg 67, 1 pg.

Board vendors turn to systems approach. Wilson, Dave, Editor; ESD, 04/88, pg 17, 2 pgs.

Buscon spotlights ASICs, standards and partnerships. Lieberman, David, Senior Editor; Computer Design, 04/01/88, pg 21, 4 pgs.

Buscon/88 West rings in a new year. Lieberman, David, Senior Editor; Mayer, John H, Senior Associate Editor; Computer Design, 02/15/88, pg 128, 2 pgs.

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Electro/88. Strassberg, Dan, Associate Editor; Computer Design, 02/15/88, pg 128, 5 pgs.

Evolutionary advances and some surprises revealed at ISSCC. Wilson, Ron, Senior Editor; Computer Design, 02/01/88, pg 21, 1 pg.

ICCAD: Logic synthesis and parallel processing. Phillips, Barry W, Technology Editor; Electronic Design, 11/12/87, pg 33, 2.5 pgs.

IEDM technical program to air key advances. Leonard, Milt, Senior Editor; Electronic Design, 11/27/87, pg 35, 3 pgs.

ISSCC announcements promise strong impact on system design. Wilson, Ron, Senior Editor; Computer Design, 04/01/88, pg 29, 2.5 pgs.

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System integration comes to the Macintosh II. Wilson, Andrew, Executive Editor; ESD, 03/88, pg 28, 1 pg.

Wescon/87. Strassberg, Dan, Associate Editor; EDN, 11/12/87, pg 139, 3.5 pgs.

Connectors

Fiber-optic connectors come down in price. O'Connell, Patricia, Managing Editor; EDN NEWS, 02/88, pg 23, 2 pgs.

Materials and hardware. Ormond, Tom, Senior Editor; EDN, 02/18/88, pg 149, 11 pgs.

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Consumer electronics

Consumer. Staff; Electronics, 01/07/88, pg 84, 2 pgs.

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In Las Vegas, the action's in three-inch CDs. Iversen, Wesley R, News Bureau—Chicago; Electronics, 01/21/88, pg 33, 1 pg.

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Military and commercial applications demand tailored high-reliability ICs. Martin, Steven L, Contributing Editor; Computer Design, 01/15/88, pg 37, 5 pgs.

Corporate appointments/development/strategies

Betting the company on a high-priced plant. Waller, Larry, News Bureau —Los Angeles; Electronics, 04/28/88, pg 95, 1 pg.

Can U.S. chip profits pay for a new generation of fabs. Lineback, J R, Managing Editor; Electronics, 02/18/88, pg 81, 2 pgs.

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Motorola confirms RISC effort as pressure on 68000 builds. Lineback, J R, News Bureau—Dallas; Electronics, 12/17/87, pg 31, 1 pg.

Selling to the military: Is it about to get easier. Naegele, Tobias, Military/Aerospace Editor; Electronics, 03/31/88, pg 83, 3 pgs.

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Users backing Motorola's 88000 chip band together and join the RISC battle. Manuel, Tom, Managing Editor; McLeod, Jonah, Managing Editor; Electronics, 04/14/88, pg 31, 1 pg.

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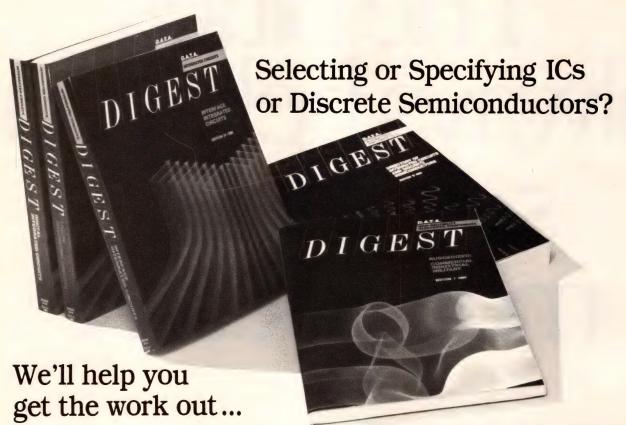
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Data communications systems/techniques

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Communications. *Staff; Electronics, 01/07/88, pg 75, 2.5 pgs.*

Computers are on the verge of the open-systems era. *Manuel, Tom, Managing Editor; Gosch, John, News Bureau—Frankfort; Electronics, 04/14/88, pg 68, 2 pgs.*

From systems to standards, the pace quickens in networking. *Runyon, Stan, Managing Editor; Electronics, 04/14/88, pg 67, 1.5 pgs.*

Software changes smart modem to smart scope. *Alunkal, John, Codex; Holley, Paul, Holley; Electronic Design, 12/10/87, pg 99, 4.5 pgs.*

The race to interconnect computer networks is on. *Curran, Lawrence, Managing Editor; Electronics, 04/14/88, pg 70, 3 pgs.*

Wide-area nets explode as standards emerge. *Shandle, Jack, New Products Editor; Electronics, 04/14/88, pg 75, 3 pgs.*

Data converters

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CD-player design requires an accurate 16-bit D/A converter. *Highton, Frederick J, Burr-Brown; EDN, 11/12/87, pg 225, 5.5 pgs.*

Converters digitize signals for DSP. *Malone, Bob, Sylvan, John, Analog Devices; EDN NEWS, 01/88, pg 24, 1 pg.*

Data capture matches flash converter speeds. *Lechner, Alexander, et al, Siemens Components; Electronic Design, 03/31/88, pg 101, 6 pgs.*

For A/D converter specs, read between the lines. *Colotti, James J, Eaton; Electronic Products, 04/15/88, pg 53, 5.5 pgs.*

Improve converter resolution with µP tracking techniques. *Carlson, Brian, Hootman, Joe, University of North Dakota; Electronic Design, 02/04/88, pg 97, 4.5 pgs.*

Make programmable sine oscillator from quad DAC chip. *Wong, James, Precision Monolithics; Electronic Design, 02/04/88, pg 103, 3.5 pgs.*

Mixed process technologies drive D-A converters to higher performance. *Mayer, John H, Senior Associate Editor; Computer Design, 03/01/88, pg 63, 4 pgs.*

One-chip ADCs reach 2 GHz; others hit 18-bit accuracy. *Runyon, Stan, Special Projects Editor; Electronics, 02/18/88, pg 77, 1 pg.*

Programmable-delay ICs control system timing. *Hilton, Craven, Barrow, Jeff, Analog Devices; EDN, 02/18/88, pg 209, 7.5 pgs.*

S/H amp-ADC matrimony provides accurate sampling. *Little, Al, Burnett, Bob, Harris; EDN, 02/04/88, pg 153, 12 pgs.*

Special Report: High-resolution arrives for ADC chips and hybrids. *Riezenman, Mike, Contributing Editor; Electronics, 01/07/88, pg 133, 6 pgs.*

Understand CMOS flash ADCs to apply them effectively. *Demler, Michael J, Datel; EDN, 01/21/88, pg 127, 6.5 pgs.*

Data processing

Data processing. *Staff; Electronics, 01/07/88, pg 65, 4 pgs.*

Desktop computers

PS/2 products proliferate. *Lewis, Sasha, Northwestern Editor; Tuck, Barbara, Associate Editor; Electronic Products, 12/15/87, pg 15, 1.5 pgs.*

Development systems

Development systems evolve toward integrated, host-independent solutions. *Falk, Howard, Contributing Editor; Computer Design, 04/01/88, pg 44, 6 pgs.*

PC-based emulators gain performance edge. *Goering, Richard, Senior Editor; Computer Design, 02/01/88, pg 26, 2 pgs.*

Digital multimeters (DMMs)

DMM adopts varied guises. *Jessen, Kenneth, Hewlett-Packard; EDN NEWS, 02/88, pg 1, 1 pg.*

High-performance DMMs and calibrators bring standards-lab specs to the benchtop. *Strassberg, Dan, Associate Editor; EDN, 02/04/88, pg 57, 6.5 pgs.*

The system DMM becomes a far more powerful tool. *Berg, Rex A, Hewlett-Packard; Electronics, 03/17/88, pg 123, 4 pgs.*

Digital signal processing

A potpourri of DSP. *Bond, John, Technology Communications; ESD, 01/88, pg 67, 6 pgs.*

Analog filtering: top gun for audio. *Ambrose, John, Exar; ESD, 01/88, pg 97, 3.5 pgs.*

Building-block chips are busy widening DSP horizons. *Leonard, Milt, Senior Editor; Electronic Design, 03/31/88, pg 68, 7.5 pgs.*

DSP chip speeds VME transfer. *Cooper, John, Ironics; ESD, 03/88, pg 47, 3 pgs.*

DSP's big conference enters the real world of products. *Young, Jeremy, Managing Editor; Electronics, 03/31/88, pg 63, 1.5 pgs.*

DSPs finally find floating point. *Taylor, David, et al, Zoran; ESD, 01/88, pg 81, 3.5 pgs.*

Digital filtering: the right stuff for video. *Williams, Bob, Ampex; Prater, Jim, NCR Microelectronics; ESD, 01/88, pg 91, 3.5 pgs.*

Digital signal processing: Chips are here, but software isn't. *McLeod, Jonah, Managing Editor; Electronics, 03/31/88, pg 57, 3 pgs.*

FFT-based filter design boosts radar system's prowess. *Cox, Roger, United Technologies Microelectronics; Electronic Design, 03/31/88, pg 81, 4 pgs.*

FFT-specific chips crunch frequency-domain data. *Cormier, Denny, Senior Technical Editor; ESD, 12/87, pg 20, 1 pg.*

Novel DSP boards break through speed bottlenecks. *Phillips, Barry W, Technology Editor; Electronic Design, 02/18/88, pg 132, 13 pgs.*

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Transform your IBM PC into a 6 1/2-digit voltmeter. *Haigh, Geoffrey, Analog Devices; Electronic Design, 02/18/88, pg 119, 4 pgs.*

Discrete components, other

A different touch: force-sensing resistors. *Yaniger, Stuart, Interlink Electronics; EDN NEWS, 03/88, pg 8, 1 pg.*

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Building tomorrow's disk controller today. *Reynolds, Jim, Randall, Dave, Andromeda Systems; Electronic Products, 12/15/87, pg 47, 3.5 pgs.*

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2M-byte diskettes need special tests for quality control. *Hartke, Jerome L, Media Sciences; EDN, 03/03/88, pg 127, 6 pgs.*

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High-resolution LCD panels change demands on driver electronics. *Fenger, Carl, Muhlemann, Kurt, Philips/Faselec; EDN, 04/14/88, pg 157, 5 pgs.*

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Building cheaper active-matrix LCDs. *Iversen, Wesley R, News Bureau—Chicago; Electronics, 01/21/88, pg 38, 0.5 pgs.*

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Distributed processing

Distributed processing provides low-cost acceleration. *Goering, Richard, Senior Editor; Computer Design, 04/01/88, pg 32, 2 pgs.*

E

Engineering workstations
Portable workstations to take on functions of desktop computing. *Staff; Electronic Design, 01/07/88, pg 82, 1 pg.*
Supercomputing gives workstations a shot. *Ohr, Stephan, Executive Editor; Till, Johna, Associate Editor; Electronic Design, 04/14/88, pg 39, 3 pgs.*
Will 386-based PCs ignite a desktop CAE explosion. *Bassak, Gil, Managing Editor; Electronic Design, 02/04/88, pg 62, 7.5 pgs.*

F

Fiber optics
Fiber-optic connectors come down in price. *O'Connell, Patricia, Managing Editor; EDN NEWS, 02/88, pg 23, 2 pgs.*
Fiber-optic sensor systems move to new markets. *Coco, Donna, Staff Editor; EDN NEWS, 01/88, pg 10, 2 pgs.*
Fiber-optic transmitters and receivers enhance data-link performance. *Ormond, Tom, Senior Editor; EDN, 03/31/88, pg 57, 5 pgs.*

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Digitally programmable 1-chip filters yield lower-cost data-acquisition systems. *Fleming, Tarlton, Associate Editor; EDN, 03/17/88, pg 83, 4.67 pgs.*

Floppy-disk drives
2M-byte diskettes need special tests for quality control. *Hartke, Jerome L, Media Sciences; EDN, 03/03/88, pg 127, 6 pgs.*

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Digital signal-synthesis tools model real-world environments. *Kafadar, Karen, Hewlett-Packard; EDN, 11/12/87, pg 239, 7.5 pgs.*
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Function generators for all seasons. *Yates, Warren, Associate Editor; Electronic Products, 12/15/87, pg 42, 4 pgs.*
Signal generators will boost speed and expand versatility. *Staff; Electronic Design, 01/07/88, pg 138, 1 pg.*

G

GPIB instruments
Personal computer-based instrument control: a tale of two buses. *Nowlin, William C, Canik, Robert, National Instruments; ESD, 01/88, pg 30, 4.5 pgs.*

GaAs technology
Designing with GaAs logic. *Cates, Ron, Vitesse Semiconductor; ESD, 03/88, pg 63, 4 pgs.*
Exclusive-OR inputs give you many uses for GaAs flip-flop. *Deierling, Carl, GigaBit Logic; Electronic Design, 12/10/87, pg 59, 4.5 pgs.*
GaAs ICs begin to make inroads into silicon territory. *Andrews, Warren, Contributing Editor; Computer Design, 02/01/88, pg 37, 6 pgs.*
Gallium arsenide digital ICs complement ECL families in high-speed applications. *Gallant, John, Associate Editor; EDN, 03/03/88, pg 79, 6 pgs.*
Rockwell's design used for 8-bit GaAs processor. *Waller, Larry, News Bureau—Los Angeles; Electronics, 02/18/88, pg 74, 1 pg.*
Will ASICs propel GaAs out of its niche. *Waller, Larry, News Bureau—Los Angeles; Electronics, 02/18/88, pg 40, 0.5 pgs.*

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Programmable array serves as a controller for dynamic RAMs. *Waugh, Thomas, Xilinx; EDN, 02/18/88, pg 169, 6.5 pgs.*

Graphics boards
Video and graphics—The twain shall meet. *Lawcewicz, Tad, Wang, Robert, Imagraph; ESD, 04/88, pg 55, 2.5 pgs.*
What's new—an electronic imaging '87 review. *Wilson, Andrew, Executive Editor; ESD, 12/87, pg 17, 2 pgs.*

Graphics circuits
Chip set combo transforms images at low cost. *Mannix, Charles, Ivex; ESD, 12/87, pg 54, 4 pgs.*
Data-compression chip eases document-processing design. *Silver, David, Kofax Image Product; Williamson, James, Advanced Micro Devices; Computer Design, 11/15/87, pg 101, 3 pgs.*

Graphics chips forge high-res boards for PCs, workstations. *Mokhoff, Nicolas, Senior Editor; Electronic Design, 03/17/88, pg 62, 10 pgs.*
Graphics pipeline merges off-the-shelf and semicustom ICs. *Wilson, Ron, Senior Editor; Computer Design, 12/87, pg 25, 2 pgs.*
Picking the right computer graphics chip. *Myrvaagnes, Rodney, Associate Editor; Electronic Products, 11/15/87, pg 26, 8.5 pgs.*
Specialized processors aim at graphics, imaging jobs. *Cole, Bernard C, Managing Editor; Electronics, 02/18/88, pg 73, 1 pg.*
VGA chip sets. *Mosley, J D, Regional Editor; EDN, 03/17/88, pg 119, 6.5 pgs.*
VGA chips offer design opportunities and latest IBM compatibility. *Williams, Tom, Western Managing Editor; Computer Design, 11/15/87, pg 50, 2.5 pgs.*

Graphics systems
3D PC graphics. *Macdonald, Sarah, Matrox; ESD, 02/88, pg 53, 3.5 pgs.*
AI beefs up gray-scale correlation. *Silver, William M, Schatz, David, Cognex; ESD, 03/88, pg 89, 3 pgs.*
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Focusing on image enhancement. *Dawson, Ben, Imaging Technology; ESD, 03/88, pg 83, 3 pgs.*
Graphics supercomputers tackle real-time visualization. *Williams, Tom, Western Managing Editor; Computer Design, 03/15/88, pg 21, 2.5 pgs.*
Graphics visualization is a real eye opener. *Manuel, Tom, Managing Editor; Electronics, 03/17/88, pg 91, 2 pgs.*
In search of a PC video bus standard. *Wilson, Andrew, Executive Editor; ESD, 03/88, pg 26, 1 pg.*
Interactive image processing using X windows. *Rasure, John, et al, University of New Mexico; ESD, 12/87, pg 32, 2 pgs.*
Landscape generation: a changing perspective. *Chen, Yin-Pao, Simulator Systems; ESD, 02/88, pg 44, 4 pgs.*
Lasers and liquid crystals project large images quickly. *Stepner, David, Greyhawk Systems; ESD, 01/88, pg 47, 3 pgs.*
Manage design trade-offs in high-end graphics board. *Whitton, Mary C, Sun Microsystems; et al, Electronic Design, 03/17/88, pg 77, 7 pgs.*
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Stereoscopic 3D imaging. *Weissman, M A, Microscience; ESD, 04/88, pg 59, 4 pgs.*
Video and graphics—The twain shall meet. *Lawcewicz, Tad, Wang, Robert, Imagraph; ESD, 04/88, pg 55, 2.5 pgs.*
What color is color. *Wilson, Andrew, Executive Editor; ESD, 01/88, pg 38, 4.5 pgs.*
Windows for workstations: A menu for multitasking. *Alexander, Tom, University of Washington; et al, ESD, 03/88, pg 74, 4.5 pgs.*

H

Hardware/interconnection, other
Interconnection bottlenecks will dominate future VLSI designs. *Staff; Electronic Design, 01/07/88, pg 104, 2 pgs.*

Heat sinks/cooling devices
Cooling devices take the heat from SMDs. *Strassberg, Dan, Associate Editor; EDN, 12/10/87, pg 97, 8.5 pgs.*
Cooling high-speed ECL coventionally. *Gupta, Omkarnath R, Gupta Packaging Technologies; Edmundson, Neil, Fairchild Semiconductor; Electronic Products, 11/15/87, pg 44, 4.5 pgs.*
Materials and hardware. *Ormond, Tom, Senior Editor; EDN, 02/18/88, pg 149, 11 pgs.*

I

Imports/exports
France. *Staff; Electronics, 01/21/88, pg 74, 4 pgs.*
Italy. *Staff; Electronics, 01/21/88, pg 78, 3 pgs.*
Japan. *Staff; Electronics, 01/21/88, pg 61, 5 pgs.*
Overseas market report. *Staff; Electronics, 01/21/88, pg 59, 2 pgs.*
United Kingdom. *Staff; Electronics, 01/21/88, pg 70, 4 pgs.*
West Germany. *Staff; Electronics, 01/21/88, pg 66, 4 pgs.*

In-circuit emulators/emulation
Focus on in-circuit emulators. *Novellino, John, Associate Editor; Electronic Design, 11/12/87, pg 139, 5 pgs.*
HLL cross compilers speed 1-chip-μC software development. *Leibson, Steven H, Regional Editor; EDN, 12/24/87, pg 127, 9 pgs.*
In-circuit emulators ease development of hardware for 80386-based applications. *Strassberg, Dan, Associate Editor; EDN, 03/03/88, pg 69,*

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Industrial electronics
Industrial. *Staff; Electronics, 01/07/88, pg 86, 2 pgs.*

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Computer cards won't replace traditional instruments. *Staff; Electronic Design, 01/07/88, pg 132, 2 pgs.*
Interface turns Mac II into GPIB controller. *DeSantis, Tom, IOtech; EDN NEWS, 04/88, pg 29, 1 pg.*

Instrumentation amps
Instrumentation amps begin to challenge op amps. *Graeme, Jerald, Burr-Brown; Electronics, 04/28/88, pg 125, 4 pgs.*

Instrumentation/design aids & services/measurement, other
Personal computer-based instrument control: a tale of two buses. *Nowlin, William C, Canik, Robert, National Instruments; ESD, 01/88, pg 30, 4.5 pgs.*
Quality will be the dominant force in future circuit designs. *Staff; Electronic Design, 01/07/88, pg 150, 2 pgs.*
Test & measurement. *Staff; Electronics, 01/07/88, pg 77, 3 pgs.*
Testing will become an integral part of the design process. *Staff; Electronic Design, 01/07/88, pg 134, 1 pg.*
Versatility is a necessity for tomorrow's test instruments. *Staff; Electronic Design, 01/07/88, pg 136, 1 pg.*

Integrated circuits/semiconductor devices/circuit design, other
Opportunity knocks for new optocouplers. *Jamison, Richard, et al, Hewlett-Packard; Electronic Products, 11/01/87, pg 57, 4 pgs.*
Programmable-delay ICs control system timing. *Hilton, Craven, Barrow, Jeff, Analog Devices; EDN, 02/18/88, pg 209, 7.5 pgs.*
RISCy business. *Harbert, Tammi, Senior Editor/News; EDN NEWS, 12/87, pg 1, 1.5 pgs.*
Semiconductors. *Staff; Electronics, 01/07/88, pg 92, 4 pgs.*
Token-bus-controller interface must resolve family disparities. *Polansky, Paul, Motorola; EDN, 03/17/88, pg 167, 9.5 pgs.*

Interconnection systems
Molded circuits require attention to new design techniques. *Williams, John, ICI Electronics; EDN, 01/21/88, pg 161, 5 pgs.*
New package technology supports soaring IC and system complexity—Decade 90 Part 4. *Leibson, Steven H, Regional Editor; EDN, 04/14/88, pg 141, 8 pgs.*
VLSI and VHSIC designs push improved backplane development. *Mayer, John H, Associate Editor; Computer Design, 01/01/88, pg 84, 5 pgs.*

L

Linear circuits
Analog ICs. *Goodenough, Frank, Senior Editor; Electronic Design, 02/18/88, pg 63, 5 pgs.*
Analog arrays will boast dedicated structures such as 12-bit ADCs. *Staff; Electronic Design, 01/07/88, pg 108, 1 pg.*
Analog's major move to new markets. *Curran, Lawrence, Managing Editor; Electronics, 12/17/87, pg 79, 2 pgs.*
Create linear ASIC macros without Spice nightmares. *Orgain, Cheryl, Analog Design Tools; Electronic Design, 12/10/87, pg 77, 3 pgs.*
Evolution, not revolution, marks most future linear IC advances. *Staff; Electronic Design, 01/07/88, pg 110, 1 pg.*
Linear semicustom shifts into high gear. *Collett, Ron, Senior Technical Editor; ESD, 12/87, pg 63, 4.5 pgs.*
These chips are breaking the linear bottleneck. *Curran, Lawrence, Managing Editor; Electronics, 12/17/87, pg 61, 4 pgs.*
To avoid compromise, consider insulation resistance. *Kirsop, Doug, Keithley Instruments; Electronic Design, 02/18/88, pg 125, 3.5 pgs.*
Video op amp, line-driver IC builds high-frequency circuits. *Salerno, Carmine, Wittlinger, Hal, GE/RCA Solid State; Electronic Design, 02/04/88, pg 107, 4 pgs.*

Local-area network architecture/design/design standards
An EtherStar is born. *Chiang, Al, Fujitsu Microelectronics; ESD, 03/88, pg 52, 4.5 pgs.*
Bitbus gains support for building low-cost serial links. *Andrews, Warren, Contributing Editor; Computer Design, 02/15/88, pg 23, 2.5 pgs.*
Custom logic helps clear LAN traffic bottlenecks. *Hammer, Claire, et al, Texas Instruments; Electronic Design, 01/21/88, pg 119, 4 pgs.*
Ethernet moves to twisted-pair for easier access. *Aseo, Joseph, West Coast Technical Editor; ESD, 03/88, pg 32, 1.5 pgs.*
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Fiber optics: a winning technology for LANs. *Southard, Robert K, AMP; Electronics, 02/04/88, pg 111, 4 pgs.*
Japanese beat the pack with optical MAP. *Cohen, Charles L, News Bureau—Tokyo; Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 02/18/88, pg 32, 0.5 pgs.*
LAN chip makers grapple in a turbulent market. *Cole, Bernard C, Managing Editor; Electronics, 04/14/88, pg 87, 3 pgs.*
Networking unties OS development knot. *McCreary, Dan, ETA Systems; ESD, 02/88, pg 61, 4.5 pgs.*
System-level constraints dictate real network throughput. *Viallet, Fabian, Gespac; Computer Design, 01/15/88, pg 79, 4.5 pgs.*
The LAN war pits IBM's token ring vs. the world. *McLeod, Jonah, Managing Editor; Electronics, 04/14/88, pg 80, 2.5 pgs.*
Work-station vendors factor in connectivity. *Runyon, Stan, Managing Editor; Electronics, 04/14/88, pg 83, 2 pgs.*

Logic analyzers/analysis
Building big systems takes hardware logic analyzers. *Boyce, Doug, Tektronix; Electronics, 03/17/88, pg 131, 3.5 pgs.*
Consider logic analyzers for more than µP applications. *Conner, Doug, Regional Editor; EDN, 12/24/87, pg 55, 9.5 pgs.*
Focus on logic analyzers. *Milne, Bob, Senior Editor; Electronic Design, 11/27/87, pg 101, 6 pgs.*
Proper glitch capture requires knowledge of logic-analyzer limits. *Schweitzer, Wolfgang, Kontron Messtechnik; EDN, 01/07/88, pg 157, 5 pgs.*

Logic arrays/systems
A programmable gate array: Can it be true. *Collett, Ronald E, Senior Technical Editor; ESD, 04/88, pg 28, 1 pg.*
A walk through a state-machine architecture. *Lytle, Craig, Kopec, Stan, Altera; ESD, 04/88, pg 45, 5 pgs.*
Architectural and process enhancements deliver faster, more flexible PLDs. *Andrews, Warren, Contributing Editor; Computer Design, 01/01/88, pg 31, 7 pgs.*
Clocking subsystems pace high-performance logic. *Shuhami, Jacob, Draper, Don, Intergraph Advanced Processor; Computer Design, 11/01/87, pg 95, 4.5 pgs.*
Everything you always wanted to know about designing a 100,000-gate ASIC. *Rau, Jerry, Daspit, Tom, LSI Logic; ESD, 02/88, pg 36, 4 pgs.*
Exclusive-OR inputs give you many uses for GaAs flip-flop. *Deierling, Carl, GigaBit Logic; Electronic Design, 12/10/87, pg 59, 4.5 pgs.*
Integrated PLDs support Multibus II bus arbitration. *Khu, Arthur, Advanced Micro Devices; EDN, 01/07/88, pg 165, 7 pgs.*
Mastering PLD test aspects eases PLD system testing. *Durwood, Brian H, Data I/O; O'Donnell, Gary, National Semiconductor; Electronic Design, 02/18/88, pg 103, 5 pgs.*
New gate array gets more density with antifuses. *Cole, Bernard C, Managing Editor; Electronics, 02/18/88, pg 75, 1 pg.*
PLD architectures vie for larger share of CPU support logic. *Wilson, Ron, Senior Editor; Computer Design, 11/01/87, pg 37, 4 pgs.*
PLD design system picks chips, partitions logic. *Collett, Ronald E, Senior Technical Editor; ESD, 02/88, pg 34, 1 pg.*
PLD testing: why, when and how. *Durwood, Brian H, Data I/O; Computer Design, 04/01/88, pg 71, 5 pgs.*
PLDs: On the road to state-machine design. *Collett, Ronald E, Senior Technical Editor; ESD, 04/88, pg 34, 6.5 pgs.*
Standard logic families will be cooler, faster, easier to use. *Staff; Electronic Design, 01/07/88, pg 120, 1 pg.*
Update: High-density PLDs. *Lewis, Sasha, Northwestern Editor; Electronic Products, 01/15/88, pg 14, 2 pgs.*

M

Mainframe computers
Cray's new Y-MP will face a more powerful rival-from cray. *Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 02/18/88, pg 31, 1.5 pgs.*
Graphics supercomputers tackle real-time visualization. *Williams, Tom, Western Managing Editor; Computer Design, 03/15/88, pg 21, 2.5 pgs.*
Japan focuses on simple but fast single-processor supercomputers. *Cohen, Charles L, News Bureau—Tokyo; Electronics, 03/03/88, pg 57, 2 pgs.*
New architectures give supercomputers power to mirror reality. *Bond, John, Contributing Editor; Computer Design, 03/15/88, pg 67, 11 pgs.*
Supercomputers: The proliferation begins. *Manuel, Tom, Managing Editor; Electronics, 03/03/88, pg 51, 6 pgs.*
Supercomputing gives workstations a shot. *Ohr, Stephan, Executive Editor; Till, Johna, Associate Editor; Electronic Design, 04/14/88, pg 39, 3 pgs.*

EDN TECHNICAL-ARTICLE DATABASE

Marketing/markets/pricing

Analog's major move to new markets. *Curran, Lawrence, Managing Editor; Electronics, 12/17/87, pg 79, 2 pgs.*

Communications. *Staff; Electronics, 01/07/88, pg 75, 2.5 pgs.*

Components. *Staff; Electronics, 01/07/88, pg 98, 3 pgs.*

Consumer. *Staff; Electronics, 01/07/88, pg 84, 2 pgs.*

Data processing. *Staff; Electronics, 01/07/88, pg 65, 4 pgs.*

France. *Staff; Electronics, 01/21/88, pg 74, 4 pgs.*

Industrial. *Staff; Electronics, 01/07/88, pg 86, 2 pgs.*

Italy. *Staff; Electronics, 01/21/88, pg 78, 3 pgs.*

Japan. *Staff; Electronics, 01/21/88, pg 61, 5 pgs.*

Military & government. *Staff; Electronics, 01/07/88, pg 88, 1.5 pgs.*

Overseas market report. *Staff; Electronics, 01/21/88, pg 59, 2 pgs.*

Pushing for continued growth in 1988. *Staff; Electronics, 01/07/88, pg 63, 2 pgs.*

Semiconductors. *Staff; Electronics, 01/07/88, pg 92, 4 pgs.*

Test & measurement. *Staff; Electronics, 01/07/88, pg 77, 3 pgs.*

United Kingdom. *Staff; Electronics, 01/21/88, pg 70, 4 pgs.*

West Germany. *Staff; Electronics, 01/21/88, pg 66, 4 pgs.*

Memory controllers

Cache tag RAM chips boost speed and simplify design. *Wyland, David C, Integrated Device Technolgy; Computer Design, 11/01/87, pg 85, 6 pgs.*

Memory devices

1M-bit video RAMs offer speed for high-resolution graphics displays. *Conner, Margery S, Regional Editor; EDN, 03/31/88, pg 79, 4.67 pgs.*

A new memory technology is about to hit the market. *Weber, Samuel, Executive Editor; Electronics, 02/18/88, pg 91, 3.5 pgs.*

BiCMOS SRAM tops ECL memories. *Hochstedler, Charles, National Semiconductor; Electronic Products, 03/01/88, pg 32, 5.5 pgs.*

Cache chips score 32-bit MMU hits. *Cormier, Denny, Senior Technical Editor; ESD, 03/88, pg 21, 4 pgs.*

Cache controllers flare memory bottleneck. *Bursky, Dave, Executive Editor; Leonard, Milt, Senior Editor; Electronic Design, 03/31/88, pg 25, 5 pgs.*

Cache tag RAM chips boost speed and simplify design. *Wyland, David C, Integrated Device Technolgy; Computer Design, 11/01/87, pg 85, 6 pgs.*

Cache-memory systems benefit from on-chip solutions. *Shear, David, Regional Editor; EDN, 12/10/87, pg 245, 10 pgs.*

Calculate the MTBF of EEPROMs with on-chip error correction. *Sweetman, David, Seeq Technology; Electronic Design, 02/04/88, pg 95, 2 pgs.*

EEPROMs compete for UV-EPROM sockets. *Lewis, Sasha, Northwestern Editor; Electronic Products, 12/01/87, pg 36, 4.5 pgs.*

EEPROMs move toward higher densities, speeds. *Harbert, Tammi, Senior Editor/News; EDN NEWS, 02/88, pg 8, 2 pgs.*

Five blazing fast CMOS SRAMS are coming. *Cole, Bernard C, Managing Editor; Electronics, 03/18/88, pg 69, 1.5 pgs.*

Flash EEPROM approaches EPROM density. *Rauh, Gary, Villott, Mike, Seeq Technology; EDN NEWS, 04/88, pg 36, 1 pg.*

Handle the ninth parity bit efficiently with 8-bit EEPROMs. *Barry, Joe, CTS Fabri-Tek; Electronic Design, 02/04/88, pg 89, 3 pgs.*

High-density flash EEPROMs are about to burst on the memory market. *Lineback, J Robert, Managing Editor; Electronics, 03/03/88, pg 47, 1.5 pgs.*

Intel close to production with a 4-MBIT EPROM. *Cole, Bernard C, Managing Editor; Electronics, 02/18/88, pg 72, 1 pg.*

Memories gain in smarts, density, and speed as feature sizes shrink. *Staff; Electronic Design, 01/07/88, pg 126, 1 pg.*

Memory ICs. *Bursky, Dave, Executive Editor; Electronic Design, 02/18/88, pg 71, 7.5 pgs.*

New challenger: the ferroelectric ram. *Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 02/04/88, pg 32, 0.5 pgs.*

RAM and ROM find a home on semicustom ICs. *Steinle, Adrienne L, NCR Microelectronics; Electronic Products, 12/01/87, pg 43, 3 pgs.*

Specialty DRAMs accelerate video system performance. *Cormier, Denny, Senior Technical Editor; ESD, 04/88, pg 22, 1 pg.*

System architecture dominates design of no-wait-state cache. *Flynn, James K, Mera, Narciso, AT&T Microelectronics; EDN, 03/17/88, pg 155, 6 pgs.*

The flag's up for the 4-Mbit DRAM derby. *Chester, Michael, Southwestern Editor; Electronic Products, 01/01/88, pg 15, 1.5 pgs.*

The next wave: 16-MBIT drams from Japan. *Cole, Bernard C, Managing Editor; Electronics, 02/18/88, pg 68, 1.5 pgs.*

These ECL-compatible SRAMS combine bipolar and CMOS. *Cole, Bernard C, Managing Editor; Electronics, 02/18/88, pg 71, 1 pg.*

Wide electrical PROMs stride into 1-bit terrain. *Leonard, Milt, Senior Editor; Electronic Design, 12/10/87, pg 29, 3 pgs.*

Microcomputer buses/interfacing

BiCMOS gate arrays promise new wave of bus-driving solutions. *Andrews, Warren, Contributing Editor; Computer Design, 03/01/88,*
pg 19, 3 pgs.

Bitbus gains support for building low-cost serial links. *Andrews, Warren, Contributing Editor; Computer Design, 02/15/88, pg 23, 2.5 pgs.*

Buscon spotlights ASICs, standards and partnerships. *Lieberman, David, Senior Editor; Computer Design, 04/01/88, pg 21, 4 pgs.*

DSP chip speeds VME transfer. *Cooper, John, Ironics; ESD, 03/88, pg 47, 3 pgs.*

Expansion buses give systems room to grow. *Lieberman, Dave, Senior Editor; Computer Design, 03/15/88, pg 52, 6 pgs.*

IPI-3 subsystems meet future data storage needs. *Coulter, Bob, Intellistor; Computer Design, 01/15/88, pg 87, 4 pgs.*

Metastable-free arbitrator coordinates processors. *Siddique, Naseer, Dike, Charles, Signetics; Electronic Design, 04/14/88, pg 107, 5 pgs.*

One-chip VMEbus interface builds compact graphics board. *Willy, John, Rivoire III, Charles, SBE; Electronic Design, 03/17/88, pg 97, 4 pgs.*

Personal computer-based instrument control: a tale of two buses. *Nowlin, William C, Canik, Robert, National Instruments; ESD, 01/88, pg 30, 4.5 pgs.*

Pooling the resources of different computing systems. *Vukovic, Philip M, Larsen, Larry L, Bit 3 Computer; Electronic Products, 12/15/87, pg 37, 4 pgs.*

SCSI rivalry heats up as new controller chips vie. *McLeod, Jonah, Managing Editor; Electronics, 03/31/88, pg 79, 1 pg.*

STE Bus: ready to break into U.S. market. *Mayer, John, Senior Associate Editor; Computer Design, 03/15/88, pg 27, 1.5 pgs.*

STE Bus vies for share of US STD Bus domain. *Harold, Peter, European Editor; EDN NEWS, 04/18/88, pg 1, 1 pg.*

Serial link increases microcomputer analog output. *Artusi, Daniel, Motorola; Electronic Design, 03/03/88, pg 105, 3 pgs.*

Serial techniques expand your options for µC peripherals. *Naufel, Naji, Motorola; EDN, 02/18/88, pg 199, 6 pgs.*

Simple circuitry connects plug-in cards to NuBus. *Harvey, Audrey, National Instruments; Electronic Design, 02/18/88, pg 97, 4 pgs.*

To boost bus bandwidth, match processor and memory timing. *Miller, Lloyd, Harris Semiconductor; Electronic Design, 03/31/88, pg 107, 4.5 pgs.*

VMEbus and Multibus II mature for multiprocessing applications. *Lieberman, David, Senior Editor; Computer Design, 11/01/87, pg 25, 7 pgs.*

What's holding up the PS/2 clones. *Manuel, Tom, Managing Editor; Electronics, 04/14/88, pg 32, 1 pg.*

Microcomputers

Computer performance still climbing at unrelenting pace. *Lieberman, David, Senior Editor; Computer Design, 12/87, pg 37, 8 pgs.*

For cost/performance, partition RISC system on bus parameters. *Cates, Ron, VLSI Technology; Electronic Design, 11/12/87, pg 121, 6 pgs.*

Languages coupled with fast processors for high throughput. *Aseo, Joseph, West Coast Technical Editor; ESD, 02/88, pg 26, 1 pg.*

Macintosh II: a new breed of PC for the engineer. *Wolfe, Ron, National Instruments; Electronic Products, 02/15/88, pg 22, 5.5 pgs.*

Macintosh II: expansion boards begin to emerge. *Yates, Warren, Associate Editor; Electronic Products, 02/15/88, pg 30, 4 pgs.*

Mainframe performance on a chip will challenge large machines. *Staff; Electronic Design, 01/07/88, pg 128, 1 pg.*

Microprocessor buses

Designers seek new approaches to open I/O bottlenecks. *Wilson, Ron, Senior Editor; Computer Design, 01/15/88, pg 57, 12.5 pgs.*

Onboard kernels for VME Bus boards. *Travis, Bill, Contributing Writer; EDN NEWS, 12/87, pg 1, 1 pg.*

VME source list points the way. *Staff; Electronic Products, 03/15/88, pg 38, 5 pgs.*

Microprocessor support chips

CPU-equipped peripheral chips force partitioning decisions. *Wilson, Ron, Senior Editor; Computer Design, 11/15/87, pg 22, 2.5 pgs.*

Chip sets for PC/AT compatibles support faster µPs and shrink board size. *Conner, Margery S, Regional Editor; EDN, 11/12/87, pg 79, 4 pgs.*

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More chips join VME barrage. *Wilson, Dave, Editor; ESD, 03/88, pg 24, 1 pg.*

Newest floating-point processors blur architectural distinctions. *Wilson, Ron, Senior Editor; Computer Design, 04/15/88, pg 32, 6 pgs.*

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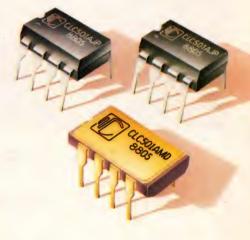
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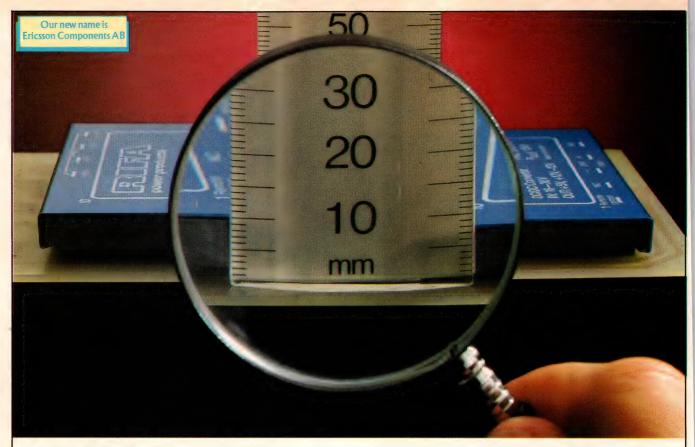
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Microprocessors

16-bit microcontrollers tune-up for real-time embedded control tasks. *Leonard, Milt, Senior Editor; Electronic Design, 03/88, pg 13, 7 pgs.*

32-bit micros: From RISC to TRON. *Myrvaagnes, Rodney, Associate Editor; Electronic Products, 04/01/88, pg 47, 3.5 pgs.*

8-bit microcontrollers specialize for embedded control applications. *Bond, John, Contributing Editor; Computer Design, 11/15/87, pg 26, 6 pgs.*

Choosing a RISC chip: What drives customers. *McLeod, Jonah, Managing Editor; Electronics, 04/28/88, pg 85, 2 pgs.*

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Designers' buying guide. *Staff; Computer Design, 02/15/88, pg 77, 39 pgs.*

Designers seek new approaches to open I/O bottlenecks. *Wilson, Ron, Senior Editor; Computer Design, 01/15/88, pg 57, 12.5 pgs.*

EDN's 14th annual µP/µC chip directory. *Cushman, Robert H, Special Features Editor; EDN, 11/26/87, pg 101, 44 pgs.*

Enhanced microcontroller chips. *Gallant, John, Associate Editor; EDN, 01/21/88, pg 113, 8.5 pgs.*

First tron microprocessor gets Japan into the 32-bit fray. *Lineback, J R, Managing Editor; Electronics, 01/21/88, pg 31, 1 pg.*

Improve converter resolution with µP tracking techniques. *Carlson, Brian, Hootman, Joe, University of North Dakota; Electronic Design, 02/04/88, pg 97, 4.5 pgs.*

Intergraph will hawk Clipper to all comers. *Curran, Lawrence, Managing Editor; Electronics, 11/12/87, pg 88, 2.5 pgs.*

MIPS gathers backers for RISC. *Lewis, Sasha, Northwestern Editor; Electronic Products, 01/01/88, pg 19, 1.5 pgs.*

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RISC processor enters the race of real-time computing. *Wilson, Ron, Senior Editor; Computer Design, 12/87, pg 23, 1.5 pgs.*

RISC slugfest: Is marketing more important than performance. *Cole, Bernard C, Managing Editor; Electronics, 04/28/88, pg 63, 6 pgs.*

RISCy business. *Harbert, Tammi, Senior Editor/News; EDN NEWS, 12/87, pg 1, 1.5 pgs.*

Rebuild a military processor to test itself for faults. *Karakotsios, Ken, Silicon Compiler Systems; Marcks, Jeff, General Dynamics; Electronic Design, 01/21/88, pg 87, 4.5 pgs.*

Rockwell's design used for 8-bit GaAs processor. *Waller, Larry, News Bureau—Los Angeles; Electronics, 02/18/88, pg 74, 1 pg.*

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The embedded processor breaks out of its niche. *Cole, Bernard C, Managing Editor; Electronics, 03/17/88, pg 61, 3 pgs.*

Military electronics

Battlefield 2000: electromagnetic guns and fiber-optic guided robots. *Staff; Electronic Design, 01/07/88, pg 146, 2 pgs.*

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Military & government. *Staff; Electronics, 01/07/88, pg 88, 1.5 pgs.*

Military ATE: capability up, tester inventory down. *Novellino, John, Associate Editor; Electronic Design, 01/21/88, pg 68, 8 pgs.*

Military and commercial applications demand tailored high-reliability ICs. *Martin, Steven L, Contributing Editor; Computer Design, 01/15/88, pg 37, 5 pgs.*

Reaching for the stars. *Wilson, Dave, Editor; ESD, 01/88, pg 22, 1 pg.*

Rebuild a military processor to test itself for faults. *Karakotsios, Ken, Silicon Compiler Systems; Marcks, Jeff, General Dynamics; Electronic Design, 01/21/88, pg 87, 4.5 pgs.*

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Minicomputers

Computer performance still climbing at unrelenting pace. *Lieberman, David, Senior Editor; Computer Design, 12/87, pg 37, 8 pgs.*

For cost/performance, partition RISC system on bus parameters. *Cates, Ron, VLSI Technology; Electronic Design, 11/12/87, pg 121, 6 pgs.*

Minisupercomputers to take over superminicomputer domain. *Staff; Electronic Design, 01/07/88, pg 80, 1 pg.*

Modems

Dial-up modem chip sets get smaller, faster. *Chester, Michael, Southwestern Editor; Electronic Products, 01/15/88, pg 22, 6 pgs.*

Single-IC modems. *Gallant, John, Associate Editor; EDN, 04/14/88, pg 119, 12 pgs.*

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Motor control circuits

Monolithic stepper-motor drivers achieve higher power levels and greater versatility. *Harold, Peter, European Editor; EDN, 01/21/88, pg 69, 8 pgs.*

Motor modeling simplifies design of control systems. *de Sa e Silva, Claudio, Unitrode; EDN, 03/31/88, pg 169, 5 pgs.*

Motor-control ICs extend performance levels of stepper and brushless dc motors. *Pryce, Dave, Associate Editor; EDN, 11/26/87, pg 61, 6 pgs.*

Motor-control semiconductors drive motor revolution. *Goodenough, Frank, Senior Editor; Electronic Design, 04/14/88, pg 78, 11 pgs.*

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Multiprocessing

VMEbus and Multibus II mature for multiprocessing applications. *Lieberman, David, Senior Editor; Computer Design, 11/01/87, pg 25, 7 pgs.*

Multiuser computer systems

Computer performance still climbing at unrelenting pace. *Lieberman, David, Senior Editor; Computer Design, 12/87, pg 37, 8 pgs.*

System-level strategy attacks key multiuser bottlenecks. *Seery, Jim, et al, AT&T; Computer Design, 01/01/88, pg 77, 6 pgs.*

N

Network analyzers/analysis

Equivalent circuits model subtle traits of advanced CMOS ICs. *Dike, Charles, Signetics; EDN, 04/14/88, pg 189, 9 pgs.*

Network architecture/design/design standards (nonlocal)

Computers are on the verge of the open-systems era. *Manuel, Tom, Managing Editor; Gosch, John, News Bureau—Frankfort; Electronics, 04/14/88, pg 68, 2 pgs.*

From systems to standards, the pace quickens in networking. *Runyon, Stan, Managing Editor; Electronics, 04/14/88, pg 67, 1.5 pgs.*

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Wide-area nets explode as standards emerge. *Shandle, Jack, New Products Editor; Electronics, 04/14/88, pg 75, 3 pgs.*

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LAN chip makers grapple in a turbulent market. *Cole, Bernard C, Managing Editor; Electronics, 04/14/88, pg 87, 3 pgs.*

MAPcon takes on factory network configuration. *Iversen, Wesley R, Industrial & Consumer Editor; Electronics, 04/14/88, pg 95, 2 pgs.*

Mainframe network chips ease big interfacing blues. *Cormier, Denny, Senior Technical Editor; ESD, 01/88, pg 17, 2 pgs.*

O

Office automation

Office automation strives to juggle competing demands. *Lieberman, David, Senior Editor; Computer Design, 11/15/87, pg 69, 9 pgs.*

Op amps

Micropower op amp offers simplicity and versatility. *Rahim, Zahid, Signetics; EDN, 01/07/88, pg 181, 7 pgs.*

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Simple techniques help you conquer op-amp instability. *Siegel, Barry L, Elantec; EDN, 03/31/88, pg 181, 8 pgs.*

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Use op amps to design optical position-sensing circuitry. *Graeme, Jerald, Burr-Brown; EDN, 11/26/87, pg 229, 7.5 pgs.*

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Erasable optical disks move out of labs. *Aseo, Joseph, West Coast Techni-*

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It's showdown time in interactive video. *Manuel, Tom, Managing Editor; Electronics, 11/26/87, pg 92, 3 pgs.*

Peripherals and memory sytems chase computer price/performance. *Williams, Tom, Western Managing Editor; Computer Design, 12/87, pg 57, 8.5 pgs.*

Optoelectronics

Advances in speed and voltage ratings enhance applications for optocouplers. *Pryce, Dave, Associate Editor; EDN, 04/28/88, pg 75, 5 pgs.*

Fiber optics: a winning technology for LANs. *Southard, Robert K, AMP; Electronics, 02/04/88, pg 111, 4 pgs.*

Fiber-optic photoelectric sensors gain in performance, popularity. *Chin, Spencer, Associate Editor; Electronic Products, 04/01/88, pg 28, 2.5 pgs.*

Fiber-optic sensor systems move to new markets. *Coco, Donna, Staff Editor; EDN NEWS, 01/88, pg 10, 2 pgs.*

Fiber-optic transmitters and receivers enhance data-link performance. *Ormond, Tom, Senior Editor; EDN, 03/31/88, pg 57, 5 pgs.*

In search of surface-mount optocouplers. *Coco, Donna, Staff Editor; EDN NEWS, 04/88, pg 3, 1 pg.*

Oscillators

Make programmable sine oscillator from quad DAC chip. *Wong, James, Precision Monolithics; Electronic Design, 02/04/88, pg 103, 3.5 pgs.*

Oscilloscopes

PC-based scopes encroach on stand-alone devices' turf. *Harbert, Tammi, Senior Editor/News; EDN NEWS, 03/88, pg 12, 1 pg.*

Productivity enhancements drive 100-MHz analog scope designs. *Mayer, John H, Associate Editor; Computer Design, 01/15/88, pg 94, 4 pgs.*

Special Report: Digital scopes are set to challenge analog units. *Riezenman, Mike, Contributing Editor; Electronics, 03/17/88, pg 107, 6 pgs.*

P

Parallel processing

Parallel processors deal with cost, programming trade-offs. *Wilson, Ron, Senior Editor; Computer Design, 11/15/87, pg 20, 2 pgs.*

Plug-in boards let your personal computer perform parallel-processing tasks. *Mosley, J D, Regional Editor; EDN, 02/04/88, pg 89, 5 pgs.*

Software will level the road for parallel processing. *Staff; Electronic Design, 01/07/88, pg 100, 1 pg.*

Parametric/functional testing

Dynamic testing describes behavior of high-frequency ADCs. *Blom, Eric D, Sipex; EDN, 04/14/88, pg 215, 8 pgs.*

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Cloning IBM's PS/2 is just the beginning. *Runyon, Stan, Special Projects; Electronics, 02/04/88, pg 34, 0.5 pgs.*

PC-based scopes encroach on stand-alone devices' turf. *Harbert, Tammi, Senior Editor/News; EDN NEWS, 03/88, pg 12, 1 pg.*

Plug-in boards let your personal computer perform parallel-processing tasks. *Mosley, J D, Regional Editor; EDN, 02/04/88, pg 89, 5 pgs.*

Plotters

Multipen plotters keep pace with CAD advancements. *Mayer, John H, Senior Associate Editor; Computer Design, 03/15/88, pg 100, 4.5 pgs.*

Power converters

DC/DC converters adapt to the needs of low-power circuits. *Sherman, Len, Maxim Integrated Products; EDN, 01/07/88, pg 145, 7 pgs.*

Growing array of 1-chip dc/dc converters provides power for diverse applications. *Pryce, Dave, Associate Editor; EDN, 02/18/88, pg 73, 5 pgs.*

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Power semiconductors

Power ICs will adapt operation to changing real-world conditions. *Staff; Electronic Design, 01/07/88, pg 112, 1 pg.*

Power MOS transistors span wide current and voltage range. *Goodenough, Frank, Senior Editor; Electronic Design, 03/88, pg 35, 3 pgs.*

Power MOSFET makes low-cost, low-dropout voltage regulator. *Hughes, Richard S, U.S. Naval Weapons Center; Electronic Design, 01/21/88, pg 115, 2 pgs.*

Smart power: Changing the face of power control. *Fury, Art, Power Integrations; Electronics, 04/28/88, pg 135, 4 pgs.*

Smart power goes off-the-shelf. *Waller, Larry, News Bureau—Los Angeles; Electronics, 12/17/87, pg 33, 0.5 pgs.*

Smart-power ICs. *Pryce, Dave, Associate Editor; EDN, 03/31/88, pg 113, 12 pgs.*

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Beware the low power factor of switch-mode power supplies. *Hansen, Arthur G, Electronic Products, 03/01/88, pg 47, 3 pgs.*

Converter makers meet reliability challenge. *Miller, George D, Editor; EDN NEWS, 03/88, pg 22, 1.5 pgs.*

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Linear regulated supplies live on. *Yates, Warren, Associate Editor; Electronic Products, 03/01/88, pg 51, 3 pgs.*

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Switcher power densities change filter-capacitor needs. *Maxwell, John, AVX; EDN, 11/12/87, pg 257, 3 pgs.*

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Switching supplies: changing with the times. *Bassett, John, Computer Products; Electronics, 01/07/88, pg 145, 4 pgs.*

Printed circuits

Improved autorouting makes old algorithm do new tricks. *Mazzullo, Tony, ECAD; Electronic Design, 04/28/88, pg 83, 3.5 pgs.*

Materials and hardware. *Ormond, Tom, Senior Editor; EDN, 02/18/88, pg 149, 11 pgs.*

Molded circuits require attention to new design techniques. *Williams, John, ICI Electronics; EDN, 01/21/88, pg 161, 5 pgs.*

PC boards hot-wired for faster, more flexible service. *Biancomano, Vincent, Components/Packaging Editor; Electronic Design, 02/18/88, pg 29, 4.5 pgs.*

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Printed-circuit processing

Materials and hardware. *Ormond, Tom, Senior Editor; EDN, 02/18/88, pg 149, 11 pgs.*

SMT changes test fixturing. *Harbert, Tammi, Senior Editor/News; EDN NEWS, 12/87, pg 24, 1.5 pgs.*

Printers

Focus on ink-jet printers: Lower prices and better printheads perk them up. *Grossman, Morris, Senior Editor; Electronic Design, 04/14/88, pg 145, 6 pgs.*

Hard-copy output moving to 3D, personal, low-cost color images. *Staff; Electronic Design, 01/07/88, pg 88, 1 pg.*

Microcapsule approach spurs filmless imaging. *Wilson, Andrew, Executive Editor; ESD, 02/88, pg 30, 1 pg.*

Printers show their colors as performance and reliability improve. *Bond, John, Contributing Editor; Computer Design, 01/01/88, pg 43, 6 pgs.*

Raster printers profit from available technologies to suit diverse uses. *Wright, Maury, Regional Editor; EDN, 01/07/88, pg 87, 5.33 pgs.*

Process control

Advanced ICs portend radical changes in system design—Decade 90 Part 1. *Leibson, Steven H, Regional Editor; EDN, 03/03/88, pg 115, 5.5 pgs.*

Processors, special-purpose (array, front-end, etc)

DSP card fits IBM PC. *Bridges, Jim, Communications Automation & Control; EDN NEWS, 03/88, pg 1, 1 pg.*

Production testing techniques

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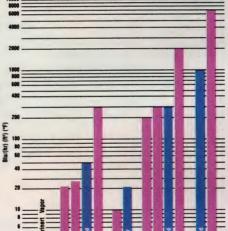
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B	125°C	−55°C	FC-40, FC-70, FC-5311	FC-77
C	150°C	−65°C	FC-40, FC-70, FC-5311	FC-77
D	200°C	−65°C	FC-70, FC-5311	FC-77
E	150°C	−195°C	FC-40, FC-70, FC-5311	Liq. N2
F	200°C	−195°C	FC-70, FC-5311	Liq. N2

GROSS LEAK TEST CONDITIONS

Military Standards	Military Approved Fluorinert Liquids		
	Indicator Fluids	Detector Fluids	Absorption Fluids
MIL-STD 883-1014	FC-40, FC-43	FC-72, FC-84	Do not apply
MIL-STD 750-1071	FC-40, FC-43	FC-72, FC-84	FC-43, FC-75, FC-77
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Specific Heat Btu/(lb.) (°F)	0.25	0.28	0.23
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S

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Acronyms from A/D to ZTAT. *Staff; Electronic Products, 11/01/87, pg 65, 11 pgs.*

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Switches
To manage fast switching jobs, look to silicone elastomers. *Stern, Harry, Conductive Rubber Technology; Electronic Design, 03/17/88, pg 123, 4.5 pgs.*

T

Technology/research, other
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V

Video
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W

Waveform analyzers/analysis
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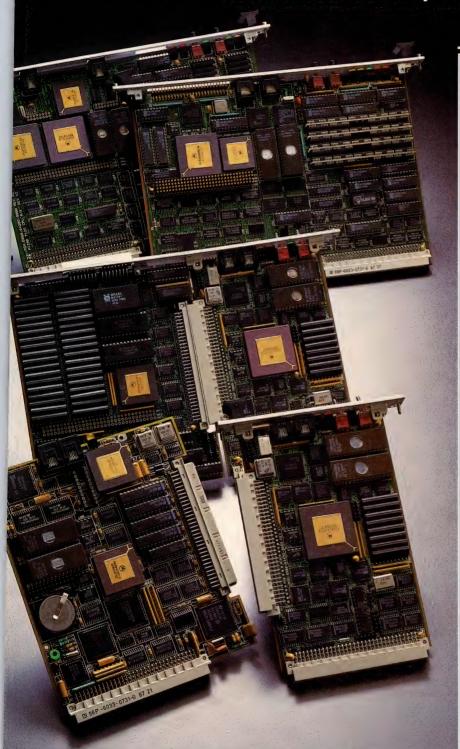
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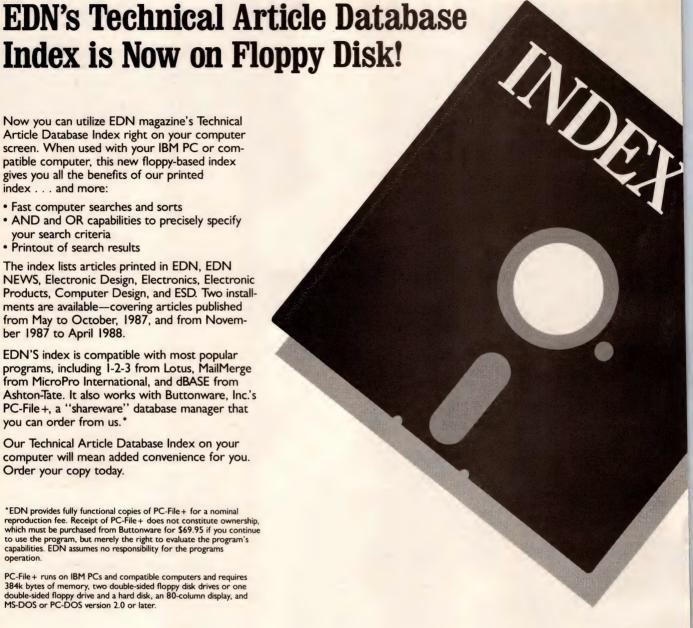
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DESIGN IDEAS

Transistor powers low-dropout regulator

James E Dekis
Maxim Integrated Products, Sunnyvale, CA
and Terry Blake
Motorola, Schaumberg, IL

The monolithic regulator chip in **Fig 1,** combined with an external pnp transistor, forms a very-low-dropout regulator. The composite regulator can supply several hundred milliamps at 5V from an input as low as 5.3V. Such low-dropout performance suits battery-powered applications, because it extends the useful life of batteries having sloping discharge curves, such as sealed lead-acid and lithium batteries.

The monolithic regulator derives its supply current from the base circuit of the external pnp transistor. The feedback-resistor ratio sets the output voltage:

$$V_{OUT} = 1.3V \times (R_1 + R_2)/R_1.$$

If the output-voltage feedback to the chip's V_{SET} input is below the bandgap-reference voltage (1.3V), the supply current into V_{IN} (the pnp transistor's base current) increases. The transistor multiplies this base current by β and delivers it to the load. The circuit's quiescent current is a function of the transistor's β and load current.

When there's no load, the quiescent current is typically 10 μA. For larger load currents, the quiescent current is simply the load current divided by the transistor's β. The regulator chip can sink 40 mA max. When you enable the chip's shut-down input, the circuit consumes 6 μA typ. R_4 supplies current to the chip under no-load conditions.
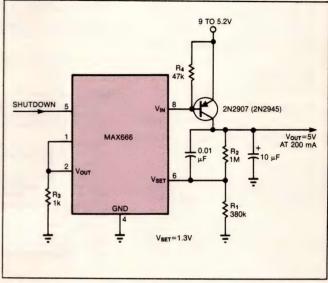
Fig 1—A monolithic regulator chip driving a dummy load sets the base current of an external, series-pass pnp transistor; the result is a very-low-dropout regulator for batteries whose output voltage droops under load.

R_3 can limit the transistor's base current. The chip's V_{OUT} pin will try to raise its voltage level to that of the V_{IN} pin when the output voltage of the chip is low. Reducing R_3 has the effect of supplying larger base currents to the external transistor.

You can substitute a 2N2945 for the 2N2907 shown in **Fig 1.** With this substitution, the circuit will supply a 5V, 100-mA max output from a 5.1V input. **EDN**

To Vote For This Design, Circle No 750

8031 routines expand address space

Robert J Ryan
Robert Merrill Inc, Tukwila, WA

This Design Idea corrects a problem with the Design Idea "Add two 16-bit pointers to the 8031 μP" (EDN, April 28, 1988, pg 238), by Noor Singh Khalsa. Khalsa uses the μP's P2 port indirectly to form the upper byte, or page, of a 16-bit address; he maintains the page

addresses in μP registers and writes the appropriate page address to P2 just prior to moving data to or from the page.

Problems arise when you attempt to use this scheme in both your main routine and a subroutine that uses a different page. Obviously, the subroutine must save the page address being used by the main routine and restore that address to P2 before returning control to

DESIGN IDEAS

the main routine. The problem is that the µP stores P2's output in a special-function register (SFR). Executing a simple read or stack push from P2 gives your subroutine the contents of P2 only when your program runs in an in-circuit emulator. In a target system, however, read and stack-push commands input the byte on P2's pins and don't input the contents of its SFR. Only read-modify-write commands that have the SFR as a destination access P2's SFR directly when your program runs in your target system.

Figs 1a and 1b show two subroutine-entry stubs that use read-modify-write instructions, DJNZ and JBC, to

```
(a)     SUB1:   PUSH    ACC             ;START SUBROUTINE
                CLR     A
        LOOP:   INC     A
                DJNZ    P2,LOOP
                MOV     P2,A            ;RESTORE P2 (OPTIONAL)
                PUSH    ACC

                  .                     ;BODY OF SUBROUTINE
                  .
                  .
                POP     P2              ;RESTORE P2 LATCH
                POP     ACC
                RET                     ;END SUBROUTINE


(b)     SUB2:   PUSH    ACC             ;START SUBROUTINE
                MOV     A,#0FFH
                JBC     P2.0,BIT1       ;BIT 0 OF P2 LATCH SET? Y-BIT1
                CLR     ACC.0
        BIT1:   JBC     P2.1,BIT2       ;BIT 1 OF P2 LATCH SET? Y-BIT2
                CLR     ACC.1
        BIT2:   JBC     P2.2,BIT3       ;BIT 2 OF P2 LATCH SET? Y-BIT3
                CLR     ACC.2
                  .
                  .                     ;CONTINUE UNTIL ALL 8 BITS TESTED
                  .
                MOV     P2,A            ;RESTORE P2 (OPTIONAL)
                PUSH    ACC             ;SAVE CONTENTS OF P2 LATCH
                  .
                  .                     ;BODY OF SUBROUTINE
                  .
                POP     P2              ;RESTORE P2 LATCH
                POP     ACC
                RET                     ;END SUBROUTINE


(c)               .
                  .
                  .
                MOV     P2RAM,#VALUE    ;LOAD RAM IMAGE WITH DESIRED VALUE
                MOV     P2,P2RAM        ;COPY RAM IMAGE TO P2 LATCH
                  .
                  .
                  .

        ;*********** SUBROUTINE ********************

                PUSH    P2RAM           ;SAVE RAM IMAGE OF P2
                  .
                  .
                  .
                POP     P2RAM           ;RESTORE RAM IMAGE OF P2
                MOV     P2,P2RAM        ;RESTORE P2 LATCH
                RET                     ;END SUBROUTINE
```

Fig 1—These three routines allow you to use an 8031's P2 special-function register to indirectly address pages of external memory in both your main routine and subroutines. The first routine (a) uses few instructions, but its execution time depends on P2's contents. The second routine (b) is faster but uses up more memory. The third routine (c) maintains a RAM image of P2's special-function register.

Novasensor accomplishes a deep sea rescue.

Place: Silicon Valley. *Date:* June 25th.
Situation: a high-tech SCUBA manufacturer, racing to beat a production deadline on a new dive computer, discovers its silicon pressure sensor is flawed. All options appear disastrous. A new vendor, Novasensor, is contacted.

Friday: design brainstormed.
Saturday: prototype fabricated.
Sunday: hybrid electronics designed.
Monday: manufacture begun.
Wednesday: testing initiated. *Saturday:* (4th of July) 100 laser-trimmed sensors delivered. Mission accomplished.

We go to any length or depth to rescue a customer in distress. Our state-of-the-art technology, experience and manufacturing resources offer the best performance and price. The Novasensor product family includes ultra-stable pressure sensors (.3 to 10,000 psi), acceleration sensors (1 to 100g), and the world's most advanced microstructures. We offer a growing number of standard products as well. To find out the depth of our expertise contact: Novasensor, 1055 Mission Court, Fremont, CA 94539. (415) 490-9100.

NOVA SENSOR

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determine the contents of P2's SFR. **Fig 1a**'s program uses few instructions, but the execution time depends on the SFR's contents; its loop can execute 255 times if P2's SFR holds FF$_{HEX}$. **Fig 1b**'s program executes more quickly, but is not very memory efficient.

Fig 1c shows an alternative scheme that employs a RAM image of P2. Every time you write a page address to P2, you also update the byte P2RAM directly. Subroutines can then push the contents of P2RAM onto the stack upon entry and restore the calling routine's page address to P2RAM and P2 upon exit. Note that you must always update P2RAM before updating P2 to ensure that the scheme in **Fig 1c** operates properly during interrupts. **EDN**

To Vote For This Design, Circle No 746

---

555 timer turns beep into warble or chirp

R E McCain
Avalon Products, Fremont, CA

The simple circuit in **Fig 1** transforms the steady beep of an audible-signal device such as a Mallory Sonalert into a distinctive warble or chirp. The value of C_2 determines just what tone color you'll get. With the 1-μF value shown, the circuit produces a warble similar to the ring tone of an inexpensive, non-Bell phone. A 10-μF value produces a chirp similar to a truck's back-up alarm. One elaboration of this circuit would be to use the second section of a 556 timer to drive a piezoelectric transducer instead of a Sonalert; that modification would vary the tone's pitch as well as the chirp rate. **EDN**

To Vote For This Design, Circle No 748
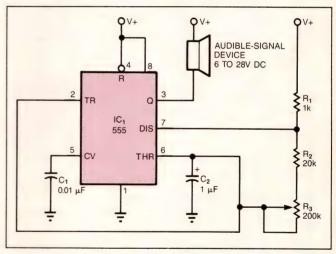
Fig 1—Adding a 555 timer to your audible-signal device's circuit will transform its plain-Jane beep into a distinctive warble or chirp.

Single-chip μP controls resolver

Tadeusz Jarosinski
FMiK ERA, Warsaw, Poland

Without the aid of external circuitry, a single-chip μP can't handle all the overhead associated with controlling a resolver. The 8253 programmable-interval-timer chips—IC$_1$ and IC$_2$ in **Fig 1a**—along with a handful of logic devices, provide sufficient speed and resolution for many applications.

The circuit in **Fig 1** lowers the single-chip μP's overhead because the μP only needs to respond to the $\overline{INT}$ signal from the motor controller, load the 8253

DESIGN IDEAS

programmable-interval timers with the appropriate divisors, and enable the timers via the START line. Normally, counter 0 of IC_1 divides the system clock (CLK) by 8. But if the single-chip μP reloads this counter for exactly one period with 16 or for two periods with 4, the drive circuit will subtract one clock pulse, or add one clock pulse, respectively (**Fig 1b**). (The single-chip μP must reload the counter with 8 immediately.) Adding or subtracting clock pulses has the effect of shifting the resolver's phase in ±4-μsec

(a)

(b)
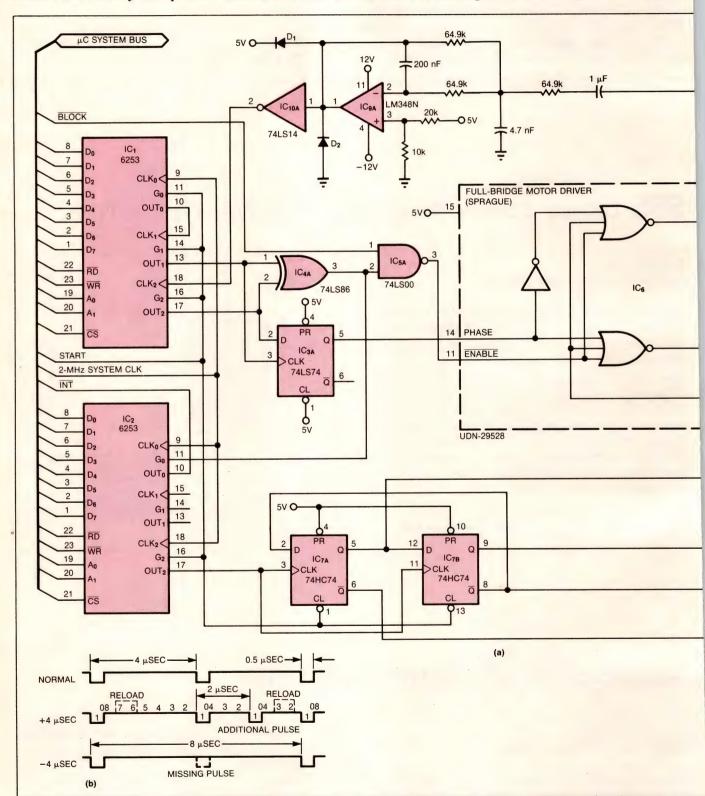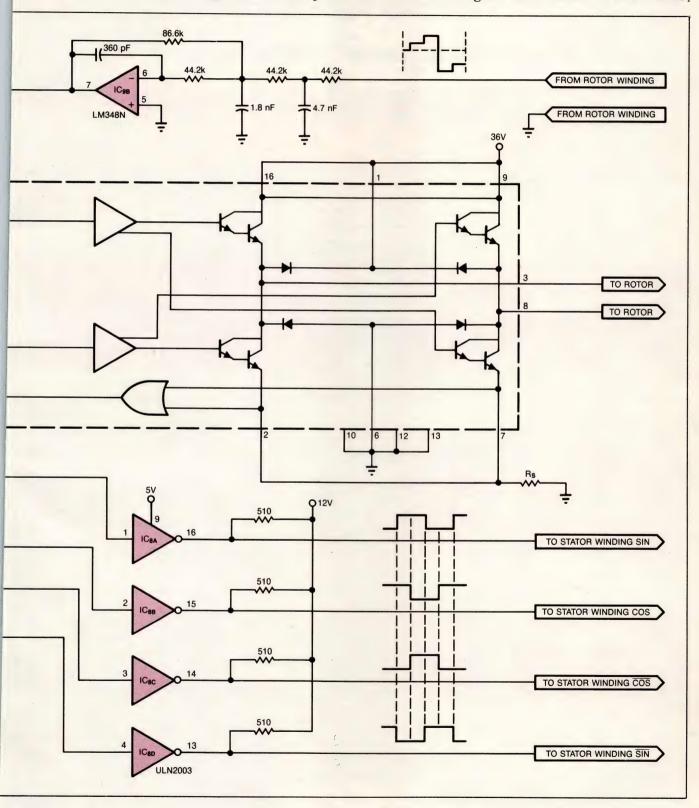
Fig 1—A single-chip μP *can control a resolver's phase in 4-μsec increments with the aid of external programmable counters and logic.*

increments.

The feedback-control portion of this design begins with the feedback signal, or error, from the resolver's rotor winding. IC_9 and IC_{10} filter this signal to a pure sinusoid and then turn it into a square wave. The phase of this square wave, with respect to the stator-drive signal, corresponds to the rotor's position. Counter 2 in IC_1 divides this square wave by 8 (mode 3). XOR gate IC_{4A} compares the divided-feedback square wave with the rotor-drive signal from counters 0 and 1 of IC_1

DESIGN IDEAS

(whose phase the single-chip µP can alter in ±4-µsec increments). Therefore, when the $\overline{\text{BLOCK}}$ signal is active high, IC_{5A} impresses the error-signal-modulated drive signal upon the motor-drive IC's Enable pin (IC_6). The width of this drive signal, in turn, determines the resolver's current.

The D flip-flop, IC_{3A}, monitors the error signal's direction (positive or negative) and controls the drive IC's $\overline{\text{PHASE}}$ input. Note that counter 0 of IC_2 can trigger the single-chip µP's interrupt line. This counter triggers an interrupt if the error signal exceeds the allowable maximum by monitoring the output of IC_{4A}. A positive transition from IC_{4A} starts the counter. Therefore, any error signal that lasts for less than half of the counter's period does not result in an interrupt.

The controller circuit's 2.5-kHz stator-drive signals result from IC_2's dividing the system clock by 200 (in mode 3). IC_7 and IC_8 develop the sine and cosine drive signals for the resolver's two stators.

The listing in **Fig 2** is for a 12-MHz 8031 single-chip µP. The major software problem to be solved is that of synchronizing the reloading of the counter with 4 at the instant that IC_1's counter 0 holds 7 or 6 (reloading with 16 is not as time critical as reloading with 4 is). The program achieves this synchronization by waiting exactly 6 µsec (until counter 0 of IC_1 contains 3 or 2) before beginning to reload the counter with 8. The 2-MHz resolver system clock is derived from the single-chip µP's 12-MHz clock; therefore, the loading of the counter and the resolver will remain synchronized (that is, the START signal ensures that the counters and flip-flops will start together), because this program ensures that two 2-µsec periods will elapse.

To synchronize the stator and rotor signals with an external event such as the closure of a limit switch, the µP must first set the $\overline{\text{BLOCK}}$ line, then incrementally shift the phase of IC_1's counter 1, and then read back the count of IC_2's counter 0 to measure the phase difference between IC_1's counters 1 and 2. **EDN**

To Vote For This Design, Circle No 749

```
00F8            U1      EQU     0FSH     ;   CS FROM UPPER 8 BITS
0003            MODE    EQU     3        ;   8253 MODE CONTROL WORD
0000            CNTO    EQU     0        ;   COUNTER 0

                                        ;   MACHINE
                                        ;   CYCLES
0000   C0A8     PHASE:  PUSH    IE       ;              SAVE STATE OF ER BIT
0002   C2AF             CLR     EA       ;              DISABLE INTERRUPTS
0004   7583F8           MOV     DPH,#U1  ;              SELECT U1 MODE RE9
0007   758203           MOV     DPL,#MODE ;
000A   E4               CLR     A        ;              SC1,SC0 : = 00
000B   F0               MOVX    @DPTR,A  ;   2          LATCH CNTO
000C   758200           MOV     DPL,#CNT0 ;  2          SELECT CNT0 (U1)
000F   E0               MOVX    A,@DPTR  ;   2          READ CNT0
0010   20E202           JB      ACC.2,V74 ;  2          JUMP, IF 7, 6, 5, 4
0013   00               NOP              ;   1
0014   00               NOP              ;   1          ADJUST 4 (2 µSEC/0.5 µSEC)
0015   30E101   V74:    JNB     ACC.1,V54 ;  2          JUMP, IF 5, 4
0018   00               NOP              ;   1          adjust 2 (1 µSEC/0.5 µSEC)
0019   00       V54:    NOP              ;   1
001A   00               NOP              ;   1
001B   500C             JNC     MIN4US   ;   2          – 4 µSEC FOR NC
001D   7404             MOV     R,#4     ;   1          4 × 0.5 µSEC = 2 – µSEC PERIOD
001F   F0               MOVX    @DPTR,A  ;   2          7 OR 6 IN CNT0 NOW
0020   00       JOIN:   NOP              ;   1
0021   00               NOP              ;   1
0022   00               NOP              ;   1          2 PERIODS ELAPSE
0023   7408             MOV     A,#8     ;   1          RETURN TO 4-µSEC PERIOD
0025   F0               MOVX    @DPTR,A  ;   2          3 OR 2 IN CNT0 NOW
0026   D0A8             POP     IE       ;              RESTORE EA
0028   22               RET

0029   7410     MIN4US: MOV     A,#16    ;   1          16 × 0.5 µSEC = 8-µSEC PERIOD
002B   F0               MOVX    @DPTR,A  ;   2          7 OR 6 IN CNT0 NOW
002C   80F2             SJMP    JOIN     ;   2          WAIT FOR 8-µSEC PERIOD

0000                    END
```

Fig 2—This program allows a 12-MHz 8031 single-chip µP to control the circuit in Fig 1.

Thermistor measures respiration rate

Ricardo Jimenez-G
San Diego State University, Calexico, CA

The circuit in **Fig 1** uses a thermistor (R_{TH}) that measures respiration rate when placed near a subject's nostril. The thermistor responds to the relatively high temperature of exhaled air. The circuit measures respiration rates between 10 and 50 breaths/sec; above and below these limits, it sounds an alarm. To measure these low-frequency phenomena, the circuit uses the
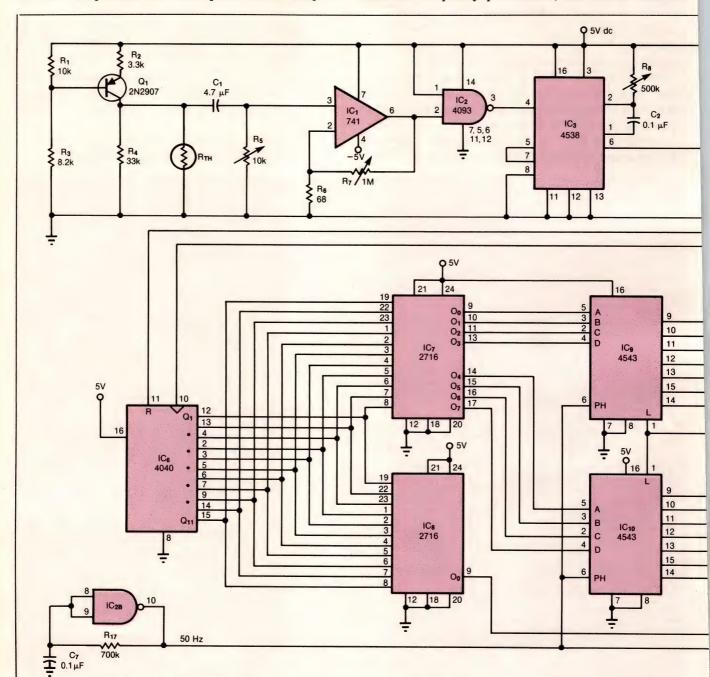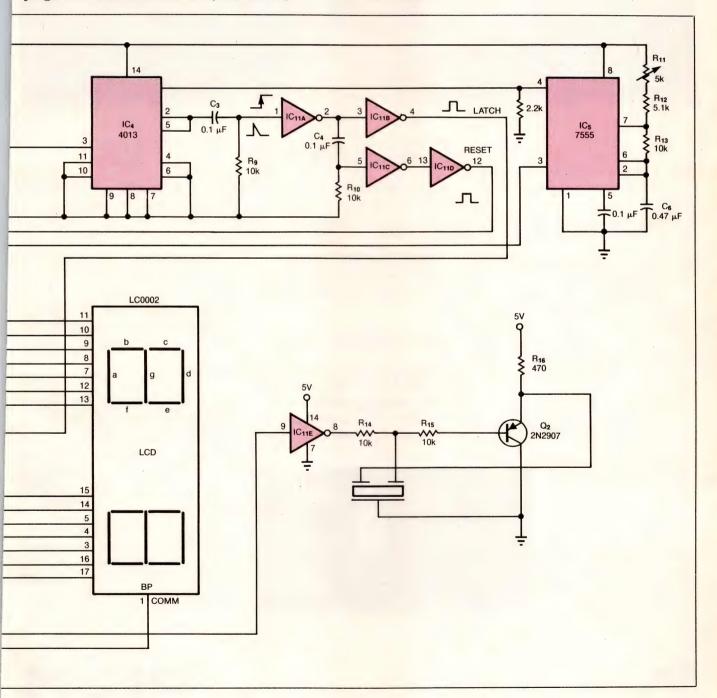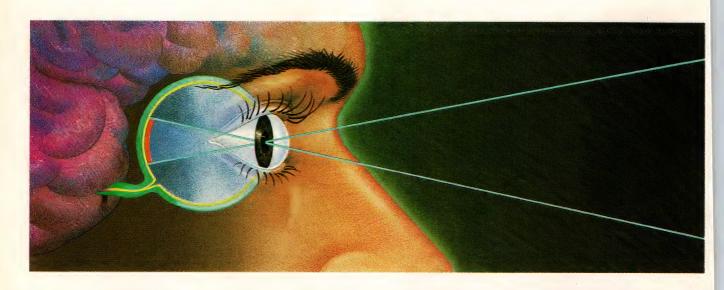
Fig 1—This circuit uses a thermistor *placed near a subject's nostril to measure respiration rate. The EPROMs translate the respiration period into rate.*

respiration signal to gate a higher-frequency multivibrator on and off. A counter totals the multivibrator's output, and a combination of EPROMs and BCD- to 7-segment decoders drives an LCD. **Fig 2** shows the programs for the two EPROMs, IC_7 and IC_8.

Q_1 and its associated circuitry compose a constant-current generator that linearizes the response of thermistor R_{TH} (Fenwal UUT43J1). R_4 is the equivalent resistance of the thermistor at 25°C. The constant current is
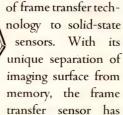
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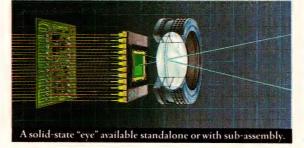
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DESIGN IDEAS

$$I_C = (V_{CC} - V_b - 0.7)/R_2$$
$$I_C = 0.62 \text{ mA}.$$

The resistance across the thermistor, therefore, equals this constant current multiplied by the parallel combination of R_4 and the thermistor. C_1 blocks dc levels from IC_1, which amplifies voltage changes arising from changes in thermistor resistance. Potentiometer R_7 adjusts IC_2's gain.

IC_2, a Schmitt trigger, triggers IC_3, which is a one-shot having a period of approximately 0.2 sec ($T = R_8 \times C_2$). The one-shot, in turn, gates on IC_5, a

multivibrator operating at 10 Hz, via flip-flop IC_4. The multivibrator drives IC_6, a 12-stage counter. IC_7 through IC_{10} form a latched decoder for the counter's output. The EPROMs, IC_7 and IC_8, convert the respiration period measured by the counter into respiration rate or trigger the out-of-range alarm, whichever is appropriate. IC_{11}'s inverter gates reset the counter and latch the display drivers.

EDN

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HEX ADDRESS	HEX DATA	HEX ADDRESS	HEX DATA	HEX ADDRESS	HEX DATA
A	60	3A	10	A	1
B	55	3B	10	B	1
C	50	3C	10	C	1
D	46	3D	10	D	1
E	43	3E	10	E	1
F	40	3F	10	F	1
10	38	40	09	10	1
11	35	41	09	11	1
12	33	42	09	12	1
13	32	43	09	13	1
14	30	44	09	14	1
15	29	45	09	15	1
16	27	46	09	16	1
17	26	47	08	17	1
18	25	48	08	18	1
19	24	49	08	19	1
1A	23	4A	08	1A	1
1B	22	4B	08	1B	1
1C	21	4C	08	1C	1
1D	21	4D	08	1D	1
1E	20	4E	08	1E	1
1F	19	4F	08	1F	1
20	19	50	08	**(b)**	
21	18	51	07		
22	18	52	07		
23	17	53	07		
24	17	54	07		
25	16	55	07		
26	16	56	07		
27	15	57	07		
28	15	58	07		
29	15	59	07		
2A	14	5A	07		
2B	14	5B	07		
2C	14	5C	07		
2D	13	5D	06		
2E	13	5E	06		
2F	13	5F	06		
30	13	60	06		
31	12	61	06		
32	12	62	06		
33	12	63	06		
34	12	64	06		
35	11				
37	11				
38	11				
39	11				

(a)

Fig 2—These EPROM programs for IC_7 (a) and IC_8 (b) effect the period-rate translations.

DESIGN IDEAS

Design Entry Blank

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Signetics Corp, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No 351

RESONANT CONTROL IC

- *Uses frequency-modulation control scheme*
- *Operates to 3 MHz*

Intended for resonant-mode power-supply control applications, the UC3860 features a frequency-modulated, fixed on-time control scheme. A precision 5V reference and a high-gain error amplifier controls a variable-frequency oscillator that operates to 3 MHz. The IC generates temperature-stable pulses as short as 200 nsec, and contains two totempole outputs for driving the gates of power MOSFETs. Each output, which you can program to run alternately or in parallel, is capable of providing 2A current pulses. The chip also provides programmable control for soft start, undervoltage lockout, and fault management. MIL-STD-883 devices will be available in a 24-pin DIP or a 28-pin LCC in December 1988. A sample-pack containing a UC3860N, a multilevel pc board, a UC3611 Schottky-diode array, and descriptive material is available for $15.
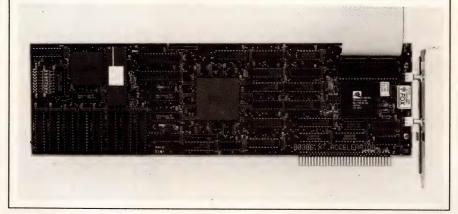
Unitrode Integrated Circuits, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410.

Circle No 352

MODEM IC

- *Suitable for use in mobile radio systems*
- *Interfaces to a µP*

The FX429 single-chip 1200-baud fast frequency-shift keying modem is targeted for use in trunked radio systems. It conforms to the UK's MPT1317/1327 Band-III trunked radio-protocol specification, but you can use it in other radio- or cable-based data-link applications. The device operates in full-duplex mode at 1200 baud. While transmitting data, you can program the device to automatically generate and transmit preamble bit-reversals for link synchronization, and a 2-byte checksum for the transmitted data. You can disable the checksum function to

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- *8088 clock rates to 10 MHz*

The EL386-88 processor/converter chip is a high-speed CMOS IC that translates the control signals and 32-bit transfer sequences of an 80386 µP into the equivalent signals and 8-bit transfer sequences of an 8088 µP. To the 80386, the EL386-88 appears as a 32-bit memory or as a peripheral device operating at a 16- to 20-MHz 80386 clock rate. To the 8-bit circuitry on the system's mother board, the El386-88 appears as an 8-bit 8088 operating at its own clock rate. The two µP clocks can be completely asynchronous, allowing the 80386 to run at a full 20 MHz, yet address peripherals designed for 4.77-MHz 8088 IBM PC data rates. The EL386-88, which increases operating speed as much as 10 times that of the 8088-based PC, automatically converts 32-bit transfer requests into multiple 8-bit transfers. The IC performs all the translation without any software changes. $50 (1000).

Edsun Laboratories Inc, 9 Spring St, Waltham, MA 02154. Phone (617) 647-9300. TLX 853664.

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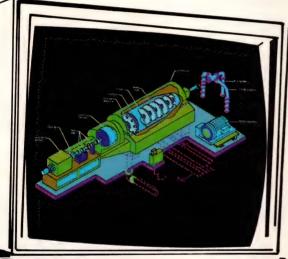
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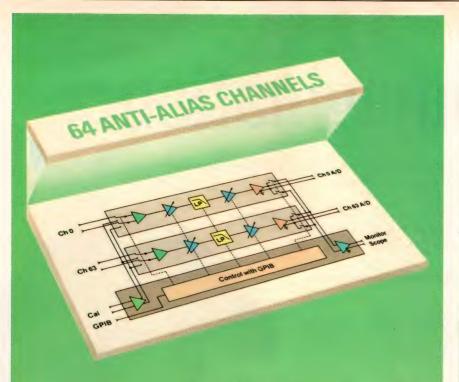
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allow continuous data transmission. In receive mode, the device detects the 16-bit Sync (control channel frame synchronization) or Synt (traffic channel frame synchronization) word that's in front of the data packet. You can also program it to error-check the data, using the transmitted checksum. The FX429 has an on-chip clock oscillator that accepts a 4.032-MHz crystal or external clock input and an 8-bit μP-compatible control/data interface. Its 1.008-MHz output drives peripheral circuitry. Fabricated in CMOS, the device operates from a 5V supply and draws a typical supply current of 5 mA when active. It is available in a 24-pin DIP or a surface-mount package. £6.78 (1000).

Consumer Microcircuits Ltd, 1 Wheaton Rd, Witham, Essex CM8 3TD, UK. Phone (0376) 513833. TLX 99382.

Circle No 354

Mx-Com Inc, 4800 Bethania Station Rd, Winston-Salem, NC 27105. Phone (919) 744-5050.

Circle No 355

NMOS CONTROLLER

- *8-bit circuitry*
- *Includes on-chip ROM*
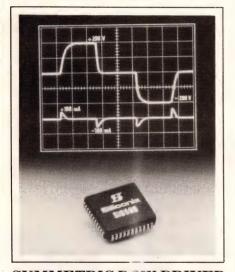
Fabricated in NMOS, the SAB 80513 8-bit, single-chip microcontroller contains 16k bytes of mask-programmable ROM. The 80513 maintains all features of the 8051 family architecture. The controller is a low-cost upgrade for designers using the SAB 8052, particularly CMOS 16k-byte ROM users whose system doesn't need the low power

INTEGRATED CIRCUITS

consumption of CMOS. In addition to the ROM, the SAB 80513 contains 256 bytes of RAM, four 8-bit ports, an interrupt structure with six vectors and two programmable priority levels, a serial channel, and oscillator and clock circuitry. The SAB 80513 comes in a 40-pin DIP and a 44-pin PLCC in both 12- and 16-MHz versions. $4.10 to $4.55 (100,000).

Siemens Components, 186 Wood Ave S, Iselin, NJ 08830. Phone (201) 321-3400.

Circle No 356
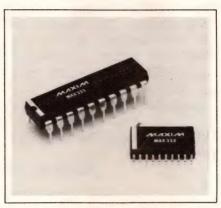
SYMMETRIC ROW DRIVER

- *For AC-TFEL displays*
- *Data-transfer rate to 4 MHz*

According to the manufacturer, the Si9560 is the first monolithic symmetric row driver to meet the requirements for ac thin-film electroluminescent (AC-TFEL) displays. Replacing two chips with one, the Si9560's symmetric drive scheme significantly reduces the differential aging effects that cause latent imaging in AC-TFEL displays, and nearly doubles the lifetime of EL displays. A front-end logic interface accepts 10.8 to 15V serial inputs and transfers data at rates to 4 MHz. Thirty-four 230V push-pull outputs on each driver provides a sink and source capability of greater than 100 mA. Although specifically designed for AC-TFEL displays, the high-

voltage, high-current outputs of the Si9560 can also drive large-area matrix vacuum-fluorescent and plasma displays. The IC is also useful for driving capacitive elements in inkjet printers. $25 (100), $5 (OEM qty, available in September).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 357

QUAD ANALOG SWITCH

- *Contains four spdt switches*
- *Low On/Off leakage current*

Designed for switching functions that require four spdt analog switches, the MAX333 operates from either single or dual supplies. Dual-supply operation ranges from ±5 to ±18V. Where ground serves as the negative source, single-supply operation ranges from 10 to 30V. The device does not require a separate 5V logic supply and is TTL/CMOS compatible. The monolithic IC can switch signals to the supply rails. At a supply voltage of ±15V, the MAX333 consumes 130 µA from the positive supply and 10 µA from the negative supply. The on-resistance is 140Ω, and the on-leakage is 0.2 nA. The off-leakage is 0.02 nA, and the turn-off time is 50 nsec. The device has break-before-make switching action. 20-pin plastic DIP $2.95; 20-pin military-grade ceramic DIP $7.90, (100).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 358

INTEGRATED CIRCUITS

GaAs MMIC

- *6- to 18-GHz bandwidth*
- *5-dB small-signal gain*

Designed for electronic-warfare applications, the HMM-11820 MMIC (monolithic microwave integrated circuit) has a small-signal gain of 5 dB over the bandwidth of 6 to 18 GHz. The chip consumes 35 mA of current and has an output power of 12 dBm at 1 dB of gain compression. The chip's VSWR is more than 2:1 at both the input and output, and the noise figure is 5.5 dB typ. The device includes dc blocking at the RF input and output, and an on-chip source bias resistor. Using a distributed topology, the chip contains four 200-μm MESFETs and all necessary capacitors, coils, and resistors. Standard wafer qualification exceeds MIL-STD-883C. $99 (1000). Production quantities are scheduled for late 1988.

Harris Microwave Semiconductor, 1530 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 433-2222.

Circle No 359

QUAD COMPARATOR
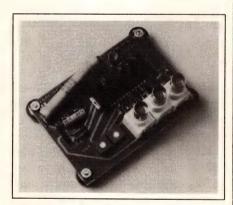
- *Input impedance is $10^{12}\Omega$*
- *Input bias current of 10 pA*

An improved version of the industry standard LM339, the ALD-4302 CMOS quad comparator features an input impedance of $10^{12}\Omega$, an input bias current of 10 pA, and a TTL-input response time of 120 nsec. The comparator can sink an output current of 60 mA, yet requires only a 150-μA supply current for each comparator. The device works from a nominal 5V supply, but will work with any single supply from 3 to 12V, or from a dual supply of 1.5 to 6V. Other features include an input voltage range that includes ground, and outputs that can sink or source current. You can use the outputs in a wired-OR connection without pull-up resistors, or in a push-pull configuration with 2 mA of sourcing current. The ALD-4302 is also a standard cell in the company's linear ASIC program. The 14-pin device has the standard LM339 pinout. Plastic DIP, $2.28; military-grade ceramic DIP, $4; small-outline package, $2.80; die form, $2.28 (100).

Advanced Linear Devices, 1030 W Maude Ave, Sunnyvale, CA 94086. Phone (408) 720-8737. TWX 510-100-6588.

Circle No 360

DISPLAY DRIVER

- *50V output into 6-pF load*
- *Operates at 175 MHz*

Based on the company's QuickChip ASIC technology, the TKDD10P CRT (Z-axis) display driver can drive a 6-pF load with 50V p-p at 175 MHz. According to the company, it is the only monolithic IC capable of this performance. You can add an external impedance-matching network to extend the performance to 200 MHz. Two input connections allow either a single-ended or a differential input drive. The inputs accept RS-343 signals of ±0.714 mV p-p. By means of a 5-kΩ potentiometer, you can vary the gain linearly

Seven money saving ideas.

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Design concept saves 20%

Assembly costs cut 50%

Assembly costs cut 40%

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Assembly costs cut 15%

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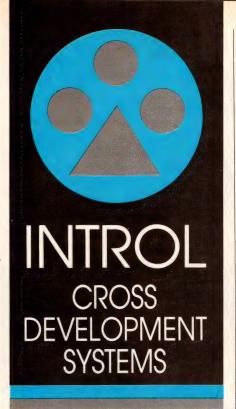
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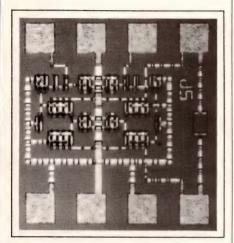
Get your FREE copy of EDN's writer's guide by circling number 800 on the Information Retrieval Service Card or by calling Sharon Gildea at (617) 964-3030.

from 0 to 80. The TKDD10P operates from a ±10V power supply and comes in a 24-pin power-tab package that features low thermal impedance. $35 (1000).

Tektronix Inc, Integrated Circuits Div, Box 14928, Portland, OR 97214. Phone (800) 835-9433, ext 100.

Circle No 361

PHASE SPLITTER

- *Operates from 10 MHz to 3 GHz*
- *2-dB typical insertion loss*

Fabricated in GaAs, the APS30010 is an active 180° phase splitter that operates to 3.5 GHz and features a single-port insertion loss of 2.0 dB typ. The chip has an amplitude balance of 0.3 dB, a phase balance of 1.0°, and a reverse isolation of 30 dB. Other features include an isolation of 20 dB min between ports, a noise figure of 12 dB, a 3-dBm compression level, and a third-order intercept point of 8 dBm. The input return loss is 20 dB typ, and the output return loss is 12 dB typ. Die form, $43.50; 8-pin flatpack, $65 (1000). Delivery, four to eight weeks ARO.

Anadigics Inc, 35 Technology Dr, Warren, NJ 07060. Phone (201) 668-5000. TWX 510-600-5741.

Circle No 362

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

DC/DC CONVERTERS

- *Available in single- and multiple-output versions*
- *Powers as many as four disk drives*
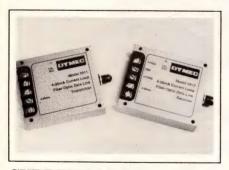
Operating from 48V inputs, these dc/dc converters can output as much as 350W. Housed in packages measuring 9×5×2.5 in., they feature a high-efficiency flux-gate switching post regulator, monocoque construction to optimize heat transfer, a current-fed inverter topology, and surface-mount technology. The open-frame converters are available in either single- (DC) or multiple-output (DCX) versions. The single-output models output from 5 to 48V at currents in the 5.5 to 30A range. The main output of some multi-output models can deliver as much as 50A of tightly regulated (1% for line and load changes) 5V power. In addition, multiple output versions feature two post-regulated mag-amp outputs and one low-power, 3-terminal regulated output. The 12V outputs have a peak current rating of 12A, enabling them to power as many as four disk drives. You can expand units to include isolation diodes and modified current-sharing for redundancy. Optional remote inhibit and dc power fail are available, as are cover/fan assemblies. $470 (100).

Todd Products Corp, 50 Emjay Blvd, Brentwood, NY 11717. Phone (516) 231-3366. TWX 510-227-4905.
Circle No 365

CURRENT LOOP

- *3200-ft transmission distance capability*
- *Solves isolation problems*

This 4- to 20-mA current-loop transmission system solves problems with erratic signals due to ground loops by using fiber-optic technology to isolate the loop and to ensure that it floats with respect to system ground. The loop has a 3200-ft transmission distance capability. The Model 5911 link transmitter accepts the current input and converts it to light. The transmitter is current-loop powered and requires no external power. The Model 5912 receiver accepts the optical signal and outputs a 4- to 20-mA output. The transmitter and receiver are housed in 2×3-in. aluminum blocks with mounting holes in the four corners. Terminal strips are provided for electrical (signal and power) inputs. Transmitter, $268; receiver, $343 (25).
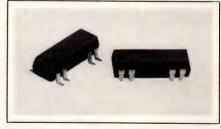
Dymec Inc, 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1511; in MA, (617) 729-7870.
Circle No 366

REED RELAYS

- *Design can withstand surface-mounting processes*
- *Offer a 10-VA max switching capability*
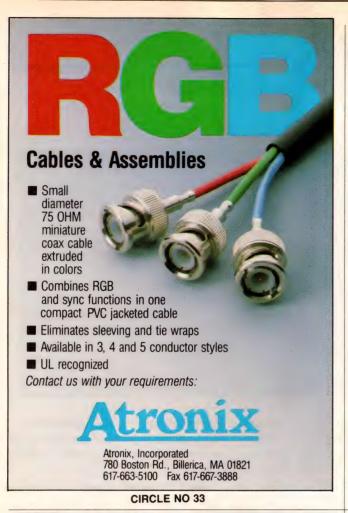
Available with gull-wing or J-hook terminals, JS2 reed relays are designed specifically for surface-mount applications. The units have a maximum switching capacity of 10W or 10 VA. Maximum voltage and current-switching ratings for the spst NO reed switch equal 100V and 0.5A, respectively. The switch will carry 1A max. Standard continuous-duty coil voltages are 5, 12, 15, and 24V dc. Initial dielectric strength is 250V dc min between open contacts and 500V dc min between the relays' coil and contacts. $3.39 (500). Delivery, stock to 10 weeks ARO.

Potter & Brumfield Inc, 200 S Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2257.
Circle No 367
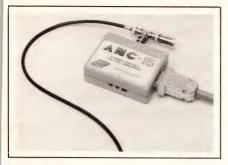
TRANSCEIVER

- *Provides an Ethernet connection to a coaxial cable*
- *Conforms to Ethernet IEEE-802.3 specifications*

The ANC-15 thin-net transceiver provides an Ethernet connection to a coaxial cable. It conforms to Ethernet/IEEE-802.3 transceiver specifications and 10M-bps Ethernet CSMA/CD operational requirements. The unit has an integrated BNC-type T-connector that facilitates the network connection. Two integral LEDs serve as SQE (heartbeat) and power indicators. The ANC-15 is housed in a compact aluminum die-cast package. $240.
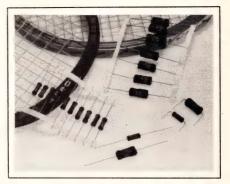
American Network Connections Inc, 462 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 737-1511.

Circle No 368

LINE CHOKES

- *Feature UL recognition*
- *Employ high-saturation core material*

The RL1283 and RL1284 Series compact power-line chokes are UL-recognized devices. The axial-lead units employ high-saturation core material, which allows them to accommodate high current levels. The chokes are available with inductance values ranging from 3.9 to 100,000 µH. Saturation-current values range from 81 mA to 15.5A. The series includes almost 100 standard

values, and nonstandard values are available. The chokes are available on tape and reel to accommodate auto-insertion equipment, or with their leads preformed to user specifications. The operating range spans −55 to +125°C. All units are supplied with insulated sleeves. MIL-STD-27D devices are also available. $0.50 (10,000). Delivery, stock to eight weeks ARO.

Renco Electronics Inc, 60 Jefryn Blvd E, Deer Park, NY 11729. Phone (516) 586-5566.

Circle No 369

INDUCTOR

- *Accommodates reflow soldering processes*
- *Available in bulk or tape-and-reel packaging*

The CM 1812 chip inductor has a ferrite core encased in a molded body made of heat-resistant resin. The core is mounted to solder-coated metal terminals, which attach to pc boards. The unit can accommodate reflow soldering processes and requires no special handling. It is available in values ranging from 0.18 to 1000 µH, and minimum Q specs at 50. From 0.18 to 8.2 µH, the standard tolerance equals ±20%; above 8.2 µH, the standard tolerance equals ±10%. The unit is available in bulk or tape-and-reel type packaging . From $0.25.

ICS Manufacturing Inc, 11661 Martens River Circle, Fountain Valley, CA 92708. Phone (800) 642-2645; in CA, (800) 247-7864.

Circle No 370

REED RELAYS

- *Feature a 1-billion cycle operating life*
- *Available in SIP and DIP housings*

These miniature mercury-wetted reed relays can switch 50W for a minimum of 1 billion cycles. Operating from a 5V supply, they consume only 125 mW. Offered in either SIPs or DIPs, the spst NO relays spec a maximum switching capability of 500V dc and 1A. Release time, over a 0- to 250-kHz frequency range, specs at 1.5 msec. The relays are available with 5, 12, or 24V dc coil-voltage ratings. Contact resistance specs at 50 mΩ. Clamp diodes are available as an option. $4.65 (500). Delivery, stock to six weeks ARO.

Gordos Corp, 1000 N Second St, Rogers, AR 72756. Phone (800) 643-3500; in AR, (501) 526-4415.

Circle No 371
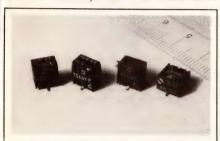
TRIMPOTS

- *Have 15-turn adjustment screws*
- *Surface-mount devices*

TS6 and TS63 Series 0.25-in. square surface-mount multiturn cermet trimmers with nominal values ≥100Ω feature a typical temperature coefficient of ±50 ppm/°C

CIRCLE NO 38

(± 100 ppm/°C maximum) over their operating temperature range of -55 to $+155$°C. Their typical contact resistance variation is 2% of their nominal value or 2Ω, and their end resistance is typically 1Ω. The TS6 version meets military specifications. The trimmers have a 15-turn mechanical rotation, and a clutch mechanism that prevents damage if you overrotate them. Four variants, with different adjustment screw and contact positions, are available. The trimmers are available in E3 Series values between 10Ω and 2.2 MΩ. The standard resistance value tolerance is $\pm 10\%$, and $\pm 5\%$ tolerance

trimmers are available on request. Their power rating is 0.25W at 85°C. TS6 Series, \$0.95; TS63 Series, \$0.73 (1000).

Sfernice, 199 blvd de la Madeleine, 06021 Nice Cedex, France. Phone 93446262. TLX 470261.

Circle No 372
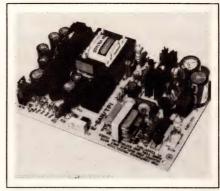
Ohmtek, 2160 Liberty Dr, Niagara Falls, NY 14304. Phone (716) 283-4025. TWX 710-524-1653.

Circle No 373

POWER SUPPLIES

- *Provide as many as four outputs*
- *UL, CSA, and VDE approved*

Low-profile (under 1 in.) ESPO22A 25W switching power supplies offer as many as four outputs that are 5 and 12V dc, and ± 5 and ± 12V dc. Available models offer dual 90-130/ 180-260V ac jumper-selectable in-

puts; a universal 90 to 260V ac input is available as an option. All models feature 0.1% line regulation. Load regulation specs at 0.5% on the main 5V output and 0.2% on all auxiliary outputs. Ripple and noise equals 1% typ. The operating range spans 0 to 50°C, and the MTBF specs at 60,000 hours. All models are UL, CSA, and VDE approved. From \$52 (100).

Total Power International Inc, 418 Bridge St, Lowell, MA 01850. Phone (617) 453-7272. TLX 948617.

Circle No 374

MOSFETs

- *Feature a fully isolated package*
- *Mount directly to heat sinks*

CPX200 Series H-Bridge HEXFET modules are designed to replace four TO-220-type power MOSFET devices in power supplies, motor-drive applications, and servo amplifiers. On-resistances spec at 0.28Ω for the 10A, 250V CPX234A module and 0.85Ω for the 5.8A, 500V CPX254A device. Both are housed in a 9-pin SIP and feature an electrically isolated base that allows you to mount the units directly to heat sinks or a chassis with only two screws or a body clip. Available options include zener-protected gates to eliminate overvoltage gate stressing, a Kelvin-connected source, and HEXSense lower switches for onboard current sensing. CPX234A, $10.82; CPX254A, $10.99 (1000). Delivery, four to six weeks.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8939.

Circle No 375

SUPPRESSORS
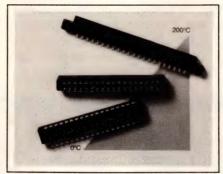
- *Pass transient voltages to ground within 5 nsec*
- *Available in 9-, 15-, 25-, and 37-position versions*

Data Line Protectors provide compact, reliable defense against data-line transient voltages that can damage computers and peripherals. These subminiature D-type protectors are a connectorized package of silicon avalanche diodes and pass any transient voltage exceeding 25V to ground in less than 5 nsec. The maximum surge power equals 2000W, and the maximum peak current measures 75A. The protectors simply plug in between the port needing protection and the appropriate cable assembly. Standard units are available in 9-, 15-, 25-, and 37-position versions. You can specify the units to protect either all or selectively loaded pins. $30 (1000). Delivery, 10 weeks ARO.

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (717) 564-0100.

Circle No 376

CARD CONNECTORS
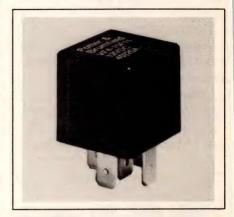
- *Withstand 200°C temperature*
- *Available in a variety of termination styles*

EB7D and EB8 dual-row edgeboard connectors are designed for high-temperature applications, including component burn-in ovens. A special high-temperature thermoset molding compound for the body and beryllium-copper material for the contacts helps them withstand 200°C operating temperatures. The connectors are available in a variety of terminations, including dip-solder, solder-eyelet, and card-extender styles. EB7D units are available with 6, 10, 12, 15, 18, 22, 36, and 43 contacts per row; EB8 connectors offer a choice of 6, 10, 12, 15, 18, 22, 24, or 25 contacts per side. EB8 connector with dual rows of 22/24 contact positions and card-extender terminations, $4.80 (1000). Delivery, four to six weeks ARO.

Dale Electronics Inc, Dept 860, Box 609, Columbus NE 68601. Phone (605) 665-9301.

Circle No 377

RELAYS

- *Can switch 40A loads*
- *Spec a 100,000 cycle lifetime*
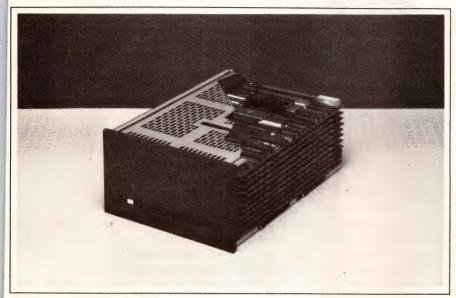
VF4 Series electromechanical relays provide a 40A switching capability in a package measuring approximately 1 in.^{3} The units are available in pc-board or socket-mount versions. The relays feature silver contacts and are available in spst NO and spdt contact configurations. Voltage-dependent maximum switching power capability ranges from 50 to 500W for dc loads and 900 VA for ac loads. The expected life, at 40A resistive, specs at 100,000 operations. Continuous-duty coils are available for 6, 12, and 24V dc operation. Nominal coil-power dissipation equals 1.6W, and initial coil-to-contact breakdown voltage equals 500V dc. Standard VF4 relays are equipped with a black plastic dust cover. Weatherproof enclosures and cases, with integral mounting brackets, are available as options. $1.33 (10,000) for an spst version. Delivery, stock to 10 weeks ARO.

Potter & Brumfield Inc, 200 S Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2272.

Circle No 378

COMPUTERS & PERIPHERALS

RAM DISKS

- *Come in full- and half-height 5¼-in. form factors*
- *SCSI-compatible units have access time of ½ msec*

The RAMstor family of RAM disks provides full- and half-height 5¼-in. form factors. Their SCSI ports can sustain a 5M-byte/sec transfer rate. The disks feature an average access time of less than ½ msec. This figure includes overhead for processing the SCSI commands. The full-height Model 5150 comes with 8M- to 80M-byte storage. The half-height Model 4150 comes with 8M- to 32M-byte capacities. You can upgrade each model in 8M-byte increments. A processor performs disk emulation, diagnostics, and error correction. It can do single-bit and multiple-bit error detection. An optional internal battery backs up 32M bytes of memory for as long as two hours. The unrecoverable data-error rate equals 1 in 10^5 power-on hours. The 8M-byte model, $6895.

Western Automation, 1700 N 55th St, Boulder, CO 80301. Phone (303) 449-6400. TWX 710-111-1401.

Circle No 380

ing at the 16M-byte capacity, the board requires 15W. The board comes with a 5-year warranty. The 2M-byte version, $1888; the 16M-byte version, $11,097.

Monolithic Systems Corp, 84 Inverness Circle E, Englewood, CO 80112. Phone (303) 790-7400. TLX 221126.

Circle No 381
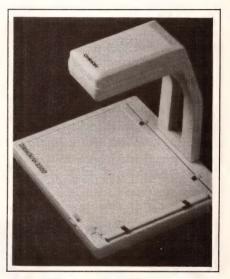
IMAGE SCANNER
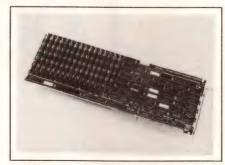
- *Has 100- to 200-dot/in. resolution in ambient light*
- *Offers optional optical-character-recognition software*

The Deskscan 2000 image scanner performs overhead scanning in ambient light conditions. The user-selectable resolution ranges from 100 to 200 dots/in. The unit weighs less than 6 lbs and consumes 15W. It provides an RS-232C with 19,200-baud communications and a bidirectional parallel interface. A configuration that includes cabling and a utility disk costs $659. For a turnkey publishing system, with PC Paintbrush+ software for an IBM PC, PC/XT, or PC/AT with at least 384k bytes of memory, the price is $695. A package with FrontPage Personal Publisher, PC Paintbrush +, TopDOS Version 3.0, and Haba

MEMORY BOARD

- *Provides 512k to 16M bytes of RAM*
- *Operates with version 4.0 of LIM/EMS specification*

The JustRAM/AT16 memory expansion board for the IBM PC/AT and compatibles contains 512k to 16M bytes of RAM, depending on the configuration. The board operates with version 4.0 of the Lotus/Intel/MicroSoft Expanded Memory Specification (LIM/EMS). With three boards you can get a 32M-byte expanded memory and 16M-byte extended memory. The board oper-

ates at 10 MHz with zero wait state and at 12 MHz with one wait state. In addition, it features switch-selectable starting addresses on 128k-byte boundaries from 0 to 16M bytes. An EMS 4.0 driver and diagnostics are standard. When operat-

Finder software costs $795. Optional optical-character-recognition software is available for an additional $895.
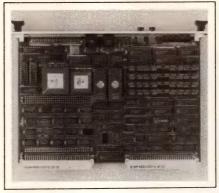
Chinon America Inc, 6374 Arizona Circle, Los Angeles, CA 90045. Phone (213) 216-7611. FAX 213-216-7646.

Circle No 382

CPU BOARD

- *Features a 68030 μP that runs up to 30 MHz*
- *Provides a 4M-byte DRAM and a 16k-byte cache memory*

The MZ7130 CPU board for the VME Bus features a 68030 μP that runs to 30 MHz. It provides a 4M-byte, dual-ported dynamic RAM with up to 2M bytes of static RAM and up to 1M byte of EPROM. In addition, the board has a 16k-byte cache memory and a memory expansion interface. At 25 MHz it oper-

ates with zero wait states. The board's I/O lines include two RS-232Cs, a SCSI port, and a parallel I/O expansion port. The board comes with a real-time clock with battery backup, an interrupt handler, an interrupt generator, and a mailbox. The board has a 32-bit master or slave interface to the bus and a system controller with four levels of arbitration. The board provides sockets for an optional 68881 or 68882 floating-point coprocessor. The software development packages

include Ready System's VRTX32, Wind River System's VxWorks, and Microware's System OS-9. $5995.

Mizar Inc, 1419 Dunn Dr, Carrollton, TX 75006. Phone (214) 446-2664. TWX 510-600-4272.

Circle No 383

A/D BOARD

- *Offers four channels for the IBM PC, PC/XT, and PC/AT*
- *Features a 12-bit A/D converter sampling at 1 MHz*

The DAS-50 A/D board provides four channels for the IBM PC, PC/XT, PC/AT and compatibles. It features a 12-bit A/D converter with a rate of 1M samples/sec max. You can trigger a series of samples with software commands, an external trigger, or a voltage level input. The board comes with a 1M-word onboard buffer memory. It employs 16 consecutive locations in the I/O

address space that you can start at any base address. It has five software-programmable, unipolar or bipolar input ranges: 0 to 5V, 0 to 10V, ±2.5V, ±5V, or ±10V. The linear-error figure specs at 1 LSB max. There are no missing codes over the full input range. A pop-up display controls the board with such features as diagnostics, memory checking, and on-line help screens. The 256k-word version, $1999; the 1M-word version, $2449.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (617) 880-3000. TLX 503989.

Circle No 384

DSP WORKSTATION
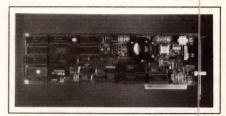
- *Has a 20-MHz 80386 μP and an 80387 coprocessor*
- *Provides a 42M-byte hard disk*

The DSP Workstation computing system employs a 20-MHz 80386 μP and a 20-MHz 80387 coprocessor. The system uses a DSP and an acquisition board based on AT&T's WE DSP32 chip and an 8-kHz codec. The system contains a 42M-byte hard-disk drive with an average access time of 28 msec; a 44M-byte tape backup; a 1.2M-byte 5¼-in. floppy-disk drive; a choice of an additional 360k- or a 720k-byte 5¼-in. floppy-disk drive; a Keytronics 101 keyboard; an NEC GB-1 EGA card; an NEC Multisync II high-resolution color monitor; a 2M-byte static RAM; and Hypersignal-Workstation DSP software. This software lets you acquire real-time data at 150 kHz to a RAM disk and at 70 kHz continuously using an

optional Data Translation 2821 or 2823 acquisition board. $9995.

Hyperception Inc, 9550 Skillman St, LB 125, Dallas, TX 75243. Phone (214) 343-8525.

Circle No 385

V.32 MODEM

- *Provides full-duplex operation at 9600 bps*
- *Has a port adapter for synchronous communications*

The Sync-Up V.32 IBM PC modem board conforms to the CCITT V.32 standard. It permits full-duplex operation at 9600 bps through the use of an echo-cancellation technique

COMPUTERS & PERIPHERALS

and a trellis-code error-correction scheme. The board features a synchronous port adpater that permits synchronous communications without a separate adapter. It runs the AT command set in asynchronous mode. This lets you use communications software such as Crosstalk, Smartcom, and MirrorII. In the synchronous mode, a Sync-Up synchronous autodialing language supports both Bisync and SDLC protocols. The board is compatible with third-party IBM 3270 and 3770 terminal emulation packages. Other features include call-progress monitoring, answer and line disconnect, an onboard speaker with volume control, and built-in diagnostics. From $1295.

Universal Data Systems, 5000 Bradford Dr, Huntsville, AL 35805. Phone (205) 721-8000. TLX 752602.
Circle No 386

CPU CARD

- *Employs a 68020 μP and 68881 math coprocessor*
- *Provides FIFO registers for message passing*

The vendor of the PG2050 32-bit computer board offers either a stand-alone, single-board computer or a CPU card for VME Bus systems. The board runs a 68020 μP and 68881 math coprocessor at 16 MHz. The sockets feature a 1M-byte max, 150-nsec, 16-bit, dual-ported static RAM. The 32-bit local memory provides a 4M-byte EPROM or a 2M-byte, zero-wait-state, static RAM and a 2M-byte EPROM. The board employs a 16-byte FIFO reg-

ister for message passing. The board offers three serial I/O ports: two are front-panel asynchronous RS-232Cs and the third provides either a synchronous/asynchronous RS-232C or an RS-485 interface to the board's two P2 connectors. In addition, the board features two 8-bit parallel I/Os, six programmable timers, and a real-time clock calendar. Gld 6000.

Philips, Industrial & Electro-acoustic Systems Div, 5600 MD Eindhoven, The Netherlands. Phone (040) 788620. TLX 35000.

Circle No 387

Philips Electronic Instruments Inc, 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800.

Circle No 388

VGA BOARD

- *Provides a 800×600-pixel mode on IBM PCs*
- *Displays 132 text columns with a 256k-byte memory*

The AST-VGA Plus VGA-adapter board for the IBM PC, PC/XT, PC/AT, and compatibles offers several graphics resolution modes. One mode provides 640×480-pixel resolution and can display 256 colors simultaneously. You can use the 800×600-pixel resolution mode with 16 simultaneously displayed colors for CAD/CAM and desktop publishing applications. In monochrome text mode, the board provides 720×400-pixel resolution with a 9×16 dot-matrix box. It displays 132 columns of text and features a 256k-byte graphics memory, but you can get up to 512k bytes. The ¾-size board is compatible with EGA, CGA, MDA, and HGC (Hercules Graphic Card) graphic standards. The board runs with the IBM 8503-, 8512-, 8513-, and 8514-compatible displays and with NEC Multisync monitors. $599.

AST Reasearch Inc, 2121 Alton Ave, Irvine, CA 92714. Phone (714) 863-9991. FAX 714-863-9478.

Circle No 389

SIEMENS

Integrated Hall circuits TLE 4901, 4902, 4903, 4910K
for the smallest magnetic air gaps

The Hall switch that goes through the eye of a needle

Miniaturization is now also showing the way to new possibilities in contactless switching. Siemens Hall ICs TLE 4901, 02 and 03 in plastic flatpacks are no more than 4.6 mm by 4.6 mm and 1.5 mm thick.

Specially suitable for the smallest magnetic air gaps are the MIKROPACK versions, which are only 0.6 mm thick.

Types TLE 4901, 4902 and 4903 are contactless static switches operated by an alternating or unipolar magnetic field. TLE 4910K generates an output voltage that is proportional to the magnetic flux density.

Siemens integrated Hall switches have proven their worth millions of times over in <u>automotive electronics – especially through their reliability even under extreme stress.</u>

With integrated protective circuits they are proof against interference and destruction and show high temperature stability of their switching points between −40 and +130°C (125°C for TLE 4902F). Shortterm operation is possible at higher temperatures.

Features like these put Hall switches at home in the most varied sectors of industrial electronics: as speed and motion sensors, as position and angle pickups or as limit switches.

In fact you'll find them
- in electronic commutation for brushless motors
- in non-contact ignition of automobiles

- in flow meters
- for measuring liquid levels
- in hydraulic intensifiers
- as acceleration sensors
- in the control of machine tools
- in floating current measurement
- throughout measurement and control engineering.

The new integrated Hall circuits from Siemens – compact high performance within tiny dimensions and with optimal functional dependability for rationalized switching concepts in endless applications.
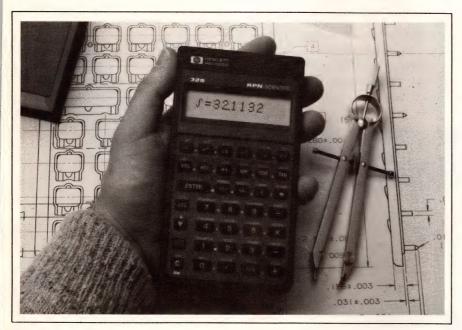
To find out more, just write Siemens AG, Infoservice 12/Z066, Postfach 23 48, D-8510 Fuerth, West Germany quoting "Integrated Hall switches".

CIRCLE NO 124

12/Z066e

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

64180, 8048, and 8049. In timing mode, you can display any 17 channels; you can expand the display as much as 16 times; and you can search for any word. In list mode, you can group 32 channels and assign them a single label. You can choose among five formats for the list-mode display. The unit includes IEEE-488, RS-232C, and Centronics interfaces; it stores data and setup information in battery-backed RAM. $2995. Delivery, 60 days ARO.

Gould Inc, 3631 Perkins Ave, Cleveland, OH 44114. Phone (800) 538-9320. TLX 196113.

Circle No 396

CALCULATOR

- *Solves equations repeatedly without re-entry*
- *Uses loops, tests, and flags to make logical decisions*

When you need to solve an equation for more than one variable, the HP-32S, RPN (reverse-Polish-notation) scientific calculator for engineering professionals saves you from having to enter an equation repeatedly. Instead of rewriting the equation to isolate the dependent variable, you simply set it equal to zero and supply values for all of the independent variables. The calculator performs numeric integration and manipulates complex numbers; it allows keystroke programming of equations for which you need repetitive solutions. The unit's 4-level stack and 27 storage registers, as well as its ability to execute program loops, to perform tests, and to use flags allow you to use it for solving problems that require logical decisions. $69.95

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

Circle No 395

MEASURING UNIT
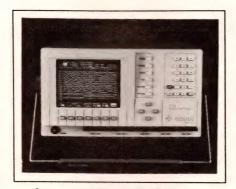
- *Adds parameter measurement to ASIC-verification tester*
- *Verifies continuity and measures impedance*

The Parametric Measuring Unit (PMU) provides an option to the vendor's STM 5200 ASIC-verification test system. Basically, the PMU is a bipolar dc source-and-measurement subsystem that can force voltage onto one or more device pins and measure the current that flows through the pin(s); or force current through a pin and measure the voltage that appears at the pin. To prevent damage to the device under test, you can separately program the forcing quantity and

LOGIC ANALYZER

- *Provides 32 25-MHz clock-rate channels*
- *Offers disassembler support for 13 μPs*

The K25 logic analyzer provides 32 channels with a 1k-word-deep capture memory for each channel. It operates with internal or external clocks at rates to 25 MHz and provides four levels of triggering with restart capability as well as event and delay counting. Disassembler
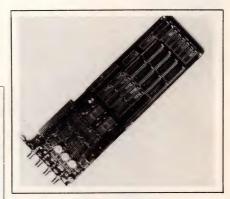
packages support the following 8- and 16-bit μPs: Z80, 6800, 8085, 8031, 8051, 8086, 8088, 68000,

the maximum permissible values of the measured quantity. If application of the programmed forcing voltage or current causes the measured quantity to exceed its programmed limits, the unit will not allow application of the full requested forcing quantity. The voltage range is −3 to 9.995V with a 4.88-mV resolution. The unit can force and measure cur-

rents from 150 pA to 100 mA in six ranges. Among other things, these capabilities permit you to use the PMU to verify continuity and measure impedance. You can also use the PMU to load a device's output and measure its maximum current-drive capability. $12,500. STM 5200, including 80386-based workstation, from $39,500.

Cadic Inc, 1725 SW 167th Pl, Beaverton, OR 97006. Phone (503) 645-2222. TLX 887936.

Circle No 397

PC-BASED SCOPE
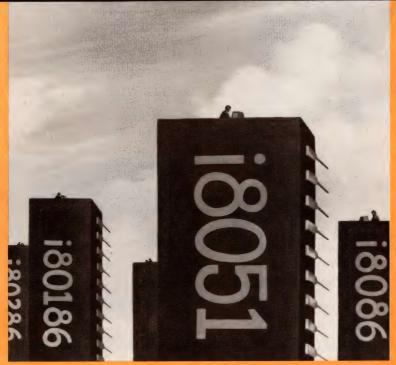
- *Can acquire 40M samples/sec*
- *Stores 256k samples in onboard RAM*

The Compuscope 220 is a single-slot board for the IBM PC bus. It allows the computer to function as a 20-MHz-bandwidth oscilloscope that simultaneously samples two analog waveforms at any of seven full-scale sensitivities from 0.1 to 10V. The board allows you to independently select the sweep rate for each channel—you can set the rate from 10 nsec to 10 sec/div. The maximum acquisition speed and acquisition-memory depth on channels A and B, respectively, are 40M and 20M samples/sec and 256k and 128k bytes. The unit stores acquired data on board—not in the computer's memory. It allows mid-, pre-, and post-triggering initiated by either channel, an external source, or a keyboard command. The software supplied performs addition, subtraction, multiplication, division, integration, and differentiation of waveforms. It also performs FFTs and curve fitting, and allows you to use the board as a digital voltmeter or a frequency counter. $1995.

Gage Applied Sciences Inc, 5905 St-François Rd, Montreal, Quebec, Canada H4S 1B6. Phone (514) 337-6893. FAX (514) 337-8411.

Circle No 398

PLD PROGRAMMER

- *Connects to PC via parallel printer port*
- *Incorporates 23 universal pin drivers*

The PLD-1100 programmer connects to an IBM PC or compatible computer through a parallel printer port. The unit, which utilizes 23 identical universal pin drivers capable of producing 0 to 25V in 100-mV steps and delivering peak currents as large as 5A, can handle nearly all programmable logic devices in 20- and 24-pin DIPs without hardware modifications or the use of personality modules. The vendor distributes device-library updates on MS-DOS-format disks. An internal µP automatically calibrates the unit, performs a number of self tests, and executes diagnostic routines. A full-screen editor allows you to edit device fuse maps, and the vector sets the programmer uses for device testing. $798.

BP Microsystems, 10681 Haddington, Suite 190, Houston, TX 77043. Phone (800) 225-2102; in TX (713) 461-9430. TLX 1561477.

Circle No 399

6½-DIGIT DMM CARD

- *Makes 250 measurements/sec*
- *Measures 5 quantities*
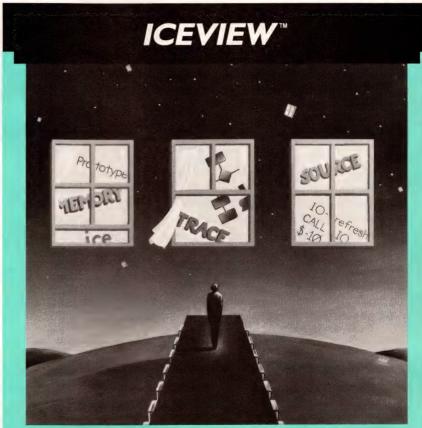
The DMM20 6½-digit multimeter on a card plugs into the vendor's PC-based modular automatic-test systems. Depending on the resolution you program, the meter will make from 0.25 to 250 measurements/sec. Quantities measured include dc and ac (true rms) voltage and current, resistance (2- or 4-wire), and the rms value of a voltage or current consisting of dc plus superimposed ac. On its most sensitive ranges, the unit can resolve 100 nV and 100 µΩ; on its least sensitive ranges, it can measure 300V rms, 500V dc, and 20 mΩ. For dc measurements on the 2V range, the error is less than 0.001% of reading plus 20 counts for 24 hours after calibration at ±1°C of calibration temperature. The unit specs ac-measurement accuracy from 20 Hz to 100 kHz: $2500. Delivery, 90 days ARO.

Summation Inc, 11335 NE 122nd Way, Kirkland, WA 98034. Phone (206) 823-8688. TLX 152219.

Circle No 400
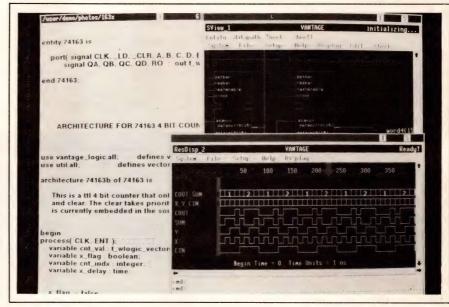
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

DESIGN VERIFIER

- *Simulator lets you perform real-time "what if?" analysis*
- *Accepts input in VHDL format and shows results of changes*

The VantageSpreadsheet lets you use VHDL (VLSI Hardware Description Language) statements to create a schematic, simulate the design's operation, and display the results in real time. You can select multiple windows for displaying your definitions. You can also display all or part of the resulting schematic and see waveforms at critical nodes. The package includes a complete implementation of the VHDL standard defined in the IEEE specification 1076. The package comes with VHDL-compatible library models. You can import schematics created by other CAE tools that use existing standards such as Unix, VHDL, and EDIF (Electronic Design Interchange Format). However, because the simulator uses incremental compiling

techniques, you can make changes on-the-fly and see the results immediately without going through time-consuming, start-up procedures such as net-list extractions. When you're satisfied with the performance of the design, you can re-export the modified schematic to your standard CAE tools for full

processing. The program runs on Apollo Domain workstations and costs $30,000 to $60,000, depending on the host's configuration.

Vantage Analysis Systems Inc, 428-40 Christy St, Suite 201, Fremont, CA 94538. Phone (415) 659-0901. FAX (415) 659-0129.

Circle No 405

IEEE-488 SOFTWARE

- *Uses command set of the HP-41 scientific calculator*
- *Has 15-digit precision*

The Eli-488 program runs on the IBM PC, PC/XT, PC/AT and compatibles. It provides engineers and scientists with calculation and control facilities that are completely compatible with the HP-41 scientific calculator. The program can use an 8087/80287 math coprocessor, if you have one in your system, and provides 15-digit precision for all calculations. If you have a National Instruments GPIB-PC interface board, you can control as many as 30 IEEE-488-based instruments. The program also includes additional functions to control I/O ports such as digital I/O boards, relay boards,

and ADCs and DACs. All HP-41 user-solution libraries are available on disk; they give you access to a range of fully debugged programs that were originally written for the HP-41. $295.

Eclipse Logic Inc, Box 2003, Huntington Park, CA 90255. Phone (213) 569-6020.

Circle No 406

DSP DESIGN TOOL

- *Lets you generate, analyze, and test a DSP design*
- *Provides an interface to board-level DSP products*

The Monarch menu-driven, DSP design tool provides a user interface with pull-down menus and on-screen help. The Design module lets you design and analyze FIR, IIR,

and Pole-zero filters with user-specified architecture and time- or frequency-domain properties. The View module lets you perform an FFT on specified files and display the result as 2- or 3-dimensional plots. The Siglab module lets you generate and analyze a wide variety of test signals and systems without leaving the main program. An applications window provides access to applications programs such as the TMS320 package. Finally, the OS Shell module lets you perform standard PC-DOS file-management operations without leaving the program. Basic Monarch package, $399.

The Athena Group Inc, 3424 NW 31st St, Gainesville, FL 32605. Phone (904) 371-2567.

Circle No 407

REAL-TIME KERNEL

- *Functions as an OS for an embedded 8051 controller system*
- *Performs task-timing and synchronization functions*

The AVRX51 real-time executive functions as an operating system in a multitasking system based on the Intel 8051 µP family. The executive provides pre-emptive scheduling for as many as eight tasks with four priority levels, three tiers of interrupt support, as many as 32 mailboxes for intertask communications, and two types of system timing services: interval timing and elapsed-time tracking. The executive provides interfaces to high-level languages such as Pascal or C; with a macroassembler you can write routines to link hardware to the executive. It comes in a relocatable object form. You can write your application programs with a cross-assembler (such as AVMAC51, which runs on the IBM PC, PC/XT, PC/AT and compatibles) and then link them to the executive for downloading to the target system. $995.

Avocet Systems Inc, 120 Union St, Rockport, ME 04856. Phone (207) 236-9055.

Circle No 408

DETAILS MANAGER

- *Shows how low-level detail meets high-level requirements*
- *Helps you meet DoD STD 2167A and other standards*

The RTrace CASE tool tracks and reports how low-level details correspond to high-level requirements in any development project. It reports and lists all requirements and their associated allocation components; components that have no requirements allocated; and requirements for which no components have been allocated. The trace reports show the relationships between requirements and the associations between high-level requirements and the low-level system components that satisfy them. You can generate a

report at any stage of the development and get a picture of the architecture or allocation. The program lets you trace requirements compliance under DoD-STD-2167A, but you can adapt it to any life-cycle methodology and use it for any development project that must meet a set of requirements and document compliances. The program runs on a VAX/VMS system (Version 4.6 or higher) that has a 4M-byte memory and that has at least 60,000 free blocks on the disk storage. Prices start at $30,000 for a single MicroVax 2000.

Nastec Corp, 24681 Northwestern Hwy, Southfield, MI 48075. Phone (313) 353-3300.

Circle No 409

Module type No. TLX-1181-G3B

When your eyes need high quality displays, you need the Toshiba ST LCD.

Once again Toshiba has made a breakthrough in display quality. Clear and beautiful displays are achieved with the ST LCD. The LCD for the new age. And for your eyes. Now, by employing a new operating mode, this module provides excellent readability from a viewing angle perpendicular to the LCD panel. This was difficult to achieve with conventional LCDs. The aim was to make our LCD easier on the eyes. We succeeded with the ST LCD. Just another improvement in the man-to-machine interface by Toshiba.

ST LCD Module Specifications

Model name	Number of dots	Dot pitch (mm)	Outline dimensions (mm)	Recommended controller	Built-in EL module
TLX-1181	640 × 400	0.35 × 0.35	276 × 168 × 12	T7779	TLX-1181-EO
TLX-1181-G3B	640 × 400	0.35 × 0.35	276 × 168 × 12	T7779	★
TLX-561	640 × 200	0.35 × 0.49	275 × 126 × 14	T7779	TLX-562-EO
TLX-1342-G3B	640 × 200	0.35 × 0.49	275 × 126 × 14	T7779	★
TLX-932	640 × 200	0.375 × 0.375	293 × 97.6 × 14	T7779	—
TLX-1241	480 × 128	0.48 × 0.48	277 × 86 × 14	T7779	—
TLX-1301V	240 × 128	0.70 × 0.70	241 × 125.3 × 12	(T6963C)	—
TLX-1013	160 × 128	0.60 × 0.60	129 × 104.5 × 14	(T6963C)	TLX-1013-EO
TLX-711A	240 × 64	0.53 × 0.53	180 × 65 × 12	(T6963C)	TLX-711A-EO
TLX-1021	120 × 64	0.48 × 0.60	85 × 70 × 20	(T6963C)	TLX-1021-EO
TLX-1391	128 × 128	0.43 × 0.43	85 × 100 × 14	(T6963C)	TLX-1391-EO
TLX-341AK	128 × 128	0.45 × 0.45	93.2 × 86.6 × 12	T6963C	—
TLX-761	640 × 64	0.38 × 0.42	320 × 47 × 14	T6963C	—

( ): Built-in controller, ★:B-ST, built-in EL module

In Touch with Tomorrow

TOSHIBA

Toshiba America, Inc., Chicago Office: 1101A Lake Cook Rd., Deerfield, IL 60015 Tel: 312-945-1500 Western Area Office: 2021 The Alameda, Suite 220, San Jose, CA 95126 Tel: 408-244-4070 Eastern Area Office: 25 Mall Road, 5th Floor, Burlington, MA 01803 Tel: 617-272-4352

CIRCLE NO 121

EDN August 4, 1988   249

252

Data book delineates applications development

The *Guide to 64180 Applications Development* gives instructions for programming the 64180 microprocessor. Its inclusion of benchmarks comparing the 64180 with other processors helps you select an appropriate CPU. It tells you how to use the μP's peripherals such as UARTs, timers, and the memory management unit, and it provides schematics and code segments that are useful in most applications. A description of hardware- and software-development environments, and a listing of support products complete the guide. A supplementary Guide Disk is also available.

Softaid Inc, 8930 Route 108, Columbia, MD 21045.

Circle No 415

Folder features timers and relays

This 8-pg publication details the vendor's line of timing controls consisting of time-delay relays and timers. The booklet provides a selection chart for time-delay relays and a timer selection guide. It also includes specifications, photographs, and diagrams.

Timeco Inc, Box 8036, Huntington, WV 25705.

Circle No 416

Summary of high-resolution graphics cards

This report identifies all manufacturers of high-resolution graphics cards for the IBM PC/AT and PS/2, and details the products they manufacture. It features a market summary, a product-evaluation scheme, and definitions of the terms used to describe the cards. This 1988 report is three times longer than the 1987 edition. $250.

Jon Peddie Associates, 6201 Asoct Dr, Oakland, CA 94611.

INQUIRE DIRECT

Booklet presents UPSs

This 28-pg illustrated brochure depicts the vendor's complete line of FerrUPS and microFerrUPS uninterruptible power systems. It provides application examples, technical and engineering specifications, information about performance and pricing, and available services and options.

Best Power Technology Inc, Box 280, Necedah, WI 54646.
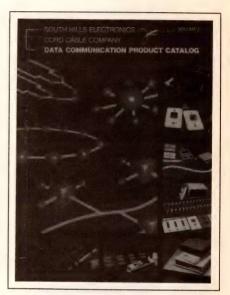
Circle No 417

Periodical deals with information management

FYI, a magazine for information management, publishes information about the company in a feature-news format that covers developments, trends, and case studies. It aims at an audience of executives in information technology; individuals who use high-technology systems, equipment, and components; and

company employees. Articles in a recent issue focus on planning strategic information networks; computerized weather forecasting; a new μP for laptop computers; fail-safe radios for emergency communications, and computerized flight simulation.

FYI, Harris Corp MS-24, 1025 W NASA Blvd, Melbourne, FL 32919.

Circle No 418

Catalog focuses on enhanced customer service

The vendor's 152-pg catalog calls attention to its enlarged customer-service sections located at three separate distribution centers in Pittsburgh, PA; Rochester, MN; and Los Angeles, CA. The publication is divided into nine parts covering coaxial and multiconductor cables, cabling systems, patch panels, cabinets, connectors, cables, converters, modems, multiplexers, power equipment, switches, and other related products for installing, expanding, or modifying computer communications systems. Specific sections on local-area networking offer coax, twinax, Ethernet, cabling system, twisted-pair, and multimode fiber-optic systems.

South Hills Electronics, 760 Beechnut Dr, Pittsburgh, PA 15205.

Circle No 419

Milt Scovill's long and winding road
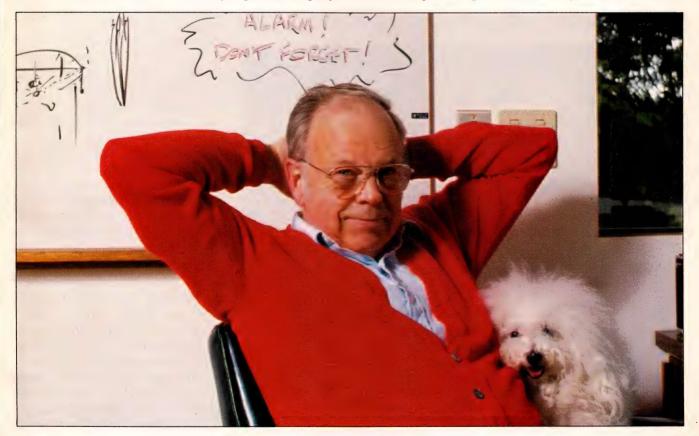
Deborah Asbrand, *Associate Editor*

Although Milt Scovill left Pacific Northwest Bell 13 years ago, the old Bell system's presence is never far away. Vestiges of what was once the world's largest company are scattered through the office that Scovill built adjacent to his Seattle, WA, home. Along a window ledge sits a row of glass insulators. Collectors items now, they once perched atop the telephone poles that remain the most visible signs of the vast Bell network. A bookshelf holds early versions of the cordless telephone and the first personal paging system, or "beeper." And mounted on the wall by the door is an old bronze plaque, a genuine Bell artifact that bears the phone company's motto: "No job is so important, no service so urgent, that we can't take time to perform our jobs safely."

In these days of fast-track careers and the pursuit of engineering as a stepping stone to marketing or management, the slow and careful immersion into engineering that the Bell system offered Scovill is long gone. So is the system itself, which

Milt Scovill parlayed an interest in radio communications and a job as a messenger boy into an engineering career. For the next 33 years, he doggedly remained an engineer first, an employee second. Now a successful consultant at age 66, he devotes all his working hours to the engineering he loves.

was his nurturer, his teacher, and, eventually, his adversary. Throughout his 33-year career at Pacific Northwest Bell, Scovill doggedly refused to acquire the notorious "Bell-shaped head" or to acquiesce to policies that he believed compromised his engineering designs. Retired from the company since 1975, he attributes his ability to command $140/hour consulting fees to the richness of his engineering experience during his long and stormy Bell career.

Ever since Pacific Telephone and Telegraph opened its Northwest operations in the 1890s, Seattle has been Bell country. Scovill's family lived across the street from Pacific Telephone's north garage, where the company's installers would go each day to sign out a truck and begin their rounds. His first association with the phone company came when he was a boy. Telephone in-

stallers paid him 25 cents to crawl beneath porches and thread the thick phone wires through holes drilled in the wooden slats.

Radio fascinated Scovill when he was a teenager, and his acquisition of amateur and commercial radio operator's licenses led to future associations with Bell that were more interesting and profitable. When he graduated from high school in 1939, Scovill, like most Seattlites, filled out a job application for the phone company. Within a short time, Pacific Telephone hired him as a messenger. For a while, he took engineering classes at the University of Washington by day and worked for the phone company at night.

After a hitch in the Navy during World War II, Scovill returned to Seattle and to his job at the phone company. When Pacific Telephone found out about his radio interest and his radio operator's licenses, it

relieved Scovill of his message-shuttling duties and transferred him to a job maintaining mobile-telephone equipment. Shortly after that, Scovill moved to the main training center, where he conducted FCC-license training classes.
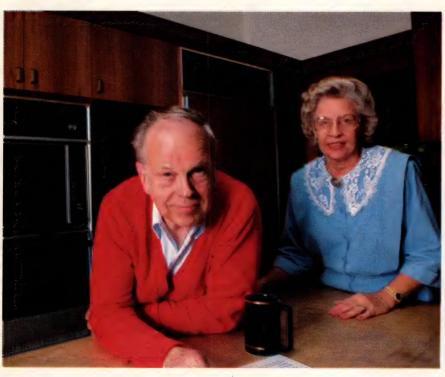
The start of a career

Scovill and Pacific Telephone quickly developed a mutual liking. The company's efforts to devise new means of communication fired his imagination, and the young man's interest and enthusiasm made him an ideal training candidate. "Opportunities kept popping up for me one after the other," he remembers. "The company put me on a rotational training program. It was an excellent program, the best learning vehicle you could find." College learning paled by comparison, he decided, and he never returned to campus.

In 1950, opportunity knocked again. "I got a call from the engineering department to work on the layout of the first microwave system in this part of the country," Scovill says. The engineers he'd been assigned to work with were "graduate engineers," he recalls, adding "I was more of a maverick than they were." First impressions aside, Scovill and the others quickly jelled into a team. His transfer to engineering, originally scheduled for just six weeks, became permanent.

Throughout the 1950s he continued to work for Pacific Telephone and remained involved in its microwave and mobile communications operations. Now married and supporting his wife and two daughters, Scovill began to think more about his financial security. He began buying into the Bell systems' stock options plan, which allowed employees to purchase shares for 85 cents on the dollar and without the assistance of a broker. "It was generous, and it was an excellent deal," he says. "Dividends were solid as a rock. You couldn't lose."

Over time, though, Scovill began

"**O**pportunities kept popping up for me one after the other. The company put me on a rotational training program. It was an excellent program, the best learning vehicle you could find."

to realize that the stock options actually carried a much higher price. It was common knowledge that Western Electric—AT&T's manufacturing arm—supplied all the parts that Pacific Telephone and the other Bell operating companies used. Stamped onto each Bell product were the words "Made by Western Electric." Scovill found some Western Electric products to be of the highest quality and the best purchase for his engineering designs. Western Electric's cable, for example, was among the best. "They could spin cable like you wouldn't believe, and build good, rugged black telephones," Scovill says. Other products, however, were less reliable, and for these items, he turned to other vendors.

The road not taken

Scovill wasn't naive. He knew that the Bell system's profits didn't come from the local-service fees that the company charged consumers. The real moneymakers were long-distance service and Western Electric. What he didn't know was how far Bell employees would go to defend the policy of purchasing only Western Electric equipment once they qualified for the company's stock plan, which gave them a financial stake in the company's prosperity. He also underestimated the amount of antipathy that his actions would arouse.

Word spread about Scovill's purchases, and at times life became difficult for him. A Pacific Telephone manager once buttonholed Scovill at a party and chastised him for appearing not to understand "how this game is played." Then, after several years of satisfaction with Scovill's performance in the microwave department, Pacific Telephone transferred him to another department. A dyed-in-the-wool company man became Scovill's new supervisor. The company's message was unmistakable: His new manager would show him how to be a true company employee.

Although he was transferred back to the microwave department two years later, Scovill's days at Bell remained "turbulent," he says. He continued to protest the mandatory Western Electric purchases. "I was under a tremendous amount of pressure." He wasn't a lone voice, however: He always had the support of his staff and his supervisor. When he's asked why he remained with the company, answers elude Scovill at first, but then he sums up his decision to stay in one word: "Stubbornness."

> **After hearing descriptions of the 1950's-era, 24-channel vacuum-tube radios used by Washington's state-police patrol, Scovill accepted the patrol's invitation to redesign the system and postponed his other plans. "It made all the old adrenaline run again."**

Indeed, Scovill turned down opportunities that others might have seized. The most tempting one came in 1958 from Bill Farinon, an engineering colleague who worked for a microwave component company. Farinon planned to start his own microwave company in the Silicon Valley area, and he was recruiting engineers to join him. He put in a call to Scovill, who turned him down. "I had just dug the hole for the foundation to this house, and Bill said 'Well, fill it in and get down here,'" Scovill recounts with a smile. His Seattle roots, however, run deep. He's a third-generation Seattlite; his grandfather was born there in 1861. Leaving, he decided, was out of the question. Undoubtedly, it was a similar resoluteness that kept him at Bell.

But in 1975, when Scovill was manager of the microwave department at Pacific Northwest Bell (the name that Pacific Telephone took on in 1965), he finally tired of the conflict. For the first time in 33 years, he laid plans that didn't include Pacific Northwest Bell. At 53, he planned to retire and finance a venture of his own, using his healthy pension to tide him over. "I had every intention of never having anything to do with the telephone business again," he says adamantly. His great love is flying, and the object of that passion for the past 25 years has been the C-2 Colonial Skimmer amphibian aircraft that he houses at Paine Field. As his first post-retirement project, he intended to manufacture and market an electronic aircraft checklist that he'd devised over the years.

A new career

A true engineer, Scovill can't resist the lure of a problem that needs solving. So when Washington's state-police patrol approached him shortly after his retirement about consulting on a microwave project, he politely explained that he was going to market his avionics device —but he kept one ear cocked. The state patrol planned to abandon its antiquated radio system in favor of a microwave system that would more efficiently link its dispatchers with its fleet of patrol cars. The patrol invited Scovill to redesign the system on a consulting basis. After hearing descriptions of the 1950s-era, 24-channel vacuum-tube radios the patrol used, Scovill caved in. "When I saw what they wanted me to do, it made all the old adrenaline run again."

Shortly after Scovill took on the state-patrol project, Oregon Public Broadcasting called to seek his services for a microwave project it had tried and failed twice to implement. Scovill paused. He hadn't planned on making consulting a second career, but he relished working on his own terms. Even more satisfying

was the fact that he could make a lot of money at it. "I started getting serious about it when my daily income from consulting was rapidly approaching my monthly pension check. I began to think maybe this wasn't a bad business to be in."

The final chapter in the relationship between Scovill and the telephone company came in 1980, when happenstance brought Scovill to the attention of two lawyers working on the Justice department's antitrust case against AT&T. The department's lawyers needed assistance in wading through the piles of technical documents associated with the case. They hired Scovill as an expert witness to decipher some of the technical material as well as AT&T's explanation of it. As he reviewed the documents, Scovill became irate. "I began to get madder and madder at the chicanery that was being played by AT&T," he says. In the spring of 1981, Scovill flew to Washington DC and recounted for the trial record the ramifications of the Bell system's parts procurement from Western Electric. His former supervisor at Pacific Northwest Bell also received a subpoena. In 1982, Judge Harold Greene ended the Bell era by ruling that the monopoly be dismembered.

Scovill's tumultuous days are behind him, and so is the corporate scene. His office now is a second-story aerie that overlooks Seattle's Lake Washington. From the room's picture window, he points out the big-leaf maples, cedars, and hawthorns. Atop his L-shaped desk are a pair of binoculars for bird watching, and a ham radio. There's also a 1917 edition of Audel's *Easy Lessons in Wireless Telegraphy* in mint condition.

Scovill, now 66, continues to handle about four consulting projects at a time—few enough to allow him to play hooky occasionally and take his aircraft for a spin. Retirement, though, is not something he considers. "I can see now that even though I'd like to do more flying, I'll never

The final chapter in Scovill's relationship with the telephone company came in 1980, when Justice department lawyers hired him as an expert witness to decipher some of the technical material involved in the department's antitrust case against AT&T.

totally retire. If I didn't enjoy what I was doing and feel that I was of value to my clients, I wouldn't do it." Not one to spend time looking back, he's unsentimental about the passing of the Bell era and the breakup of AT&T.

The 5×5-ft topographical map mounted on one of Scovill's office walls bears mute testimony to his past and present relationship with the now-defunct Bell system. Scovill had bought the map from Pacific Northwest Bell when it sold its older office furniture and other equipment after relocating to new headquarters. The map once hung in the engineering department where Scovill worked, and neat black lines on the map's surface trace the labyrinthine pattern of the company's microwave facilities throughout the northwest.

Undaunted by the magnitude of his former employer's presence, Scovill has added to the map since he acquired it. In addition to the original lines, he's plotted a second set of lines that represent his own, post-Bell microwave projects. The added lines are fewer in number than the original, but they're marked just as boldly. **EDN**

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1988 Editorial Calendar and Planning Guide

EDN

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Oct. 13	Sept. 22	Test & Measurement Special Issue, Instruments, Computers & Peripherals	Closing: Sept. 29 Mailing: Oct. 20
Oct. 27	Oct. 6	CAE, Computers & Peripherals, Integrated Circuits, Wescon '88 Show Preview	
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LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

Surveys quiz
CASE users and vendors

What do CASE-tool users want? And what do vendors think they ought to want? Strategic Focus, a consulting firm based in Milpitas, CA, interviewed 400 CASE-tool users and some of the sellers of those tools. It found that users think the tools often lack some very highly desirable features. They said that the majority of individual packages doesn't address the entire range of requirements for developing software from beginning to end. Users also wanted to see more interfaces between tools. And they wanted better integration of various tools needed throughout the development cycle, including a uniform interface to database management systems.

Learning how to use CASE tools takes too long, some users said. Others pointed out that the initial costs are high enough to require some kind of formal justification to superiors prior to purchase and a great deal of pressure to produce afterward. Users would also like better means for measuring productivity when using CASE packages. Because most of the CASE-tool companies are relatively small, support for customers at remote sites is generally very weak.

On the positive side, users identified the five top reasons why they turn to CASE tools in the first place. Of those polled, 37% said they use these tools to track the users' requirements throughout the entire development period. And 35% found that when using CASE tools, they can communicate better with end users. Among the other benefits derived from using CASE tools were improved quality of the final products, reusable software modules, and reduction in the time required

HOW USERS RATE CASE TOOLS

LIFE CYCLE PHASE	SATISFIED (%)	DISSATISFIED (%)
STRATEGIC PLANNING	30	70
ANALYSIS	65	35
DESIGN	70	30
PROTOTYPING	66	34
CODE GENERATION	50	50
DEBUGGING	54	46
PERFORMANCE TUNING	37	63
SYSTEM BUILDING	50	50
OPERATION/MAINTENANCE	50	50
DOCUMENTATION	61	39
REVERSE ENGINEERING	0	100
PROJECT MANAGEMENT	50	50
CONFIGURATION MANAGEMENT	46	54
SOURCE CODE CONTROL	50	50

(SOURCE: STRATEGIC FOCUS)

to complete a given project.

When Strategic Focus surveyed the vendors themselves, it found them fairly aware of the relative importance of various features and services that will be keys to their success in the next few years. They said they considered customer education and support very significant. They also believe that it's good to include in the packages ways to measure improved productivity. Building and maintaining a strong

direct sales force and establishing a strong company image are also critical. Strategic Focus sees a major shakedown coming in the CASE-tool marketplace, and it predicts that, of the more than 55 CASE vendors currently vying for market share in the US, it's very possible that only a third of them will still be around in 1991.
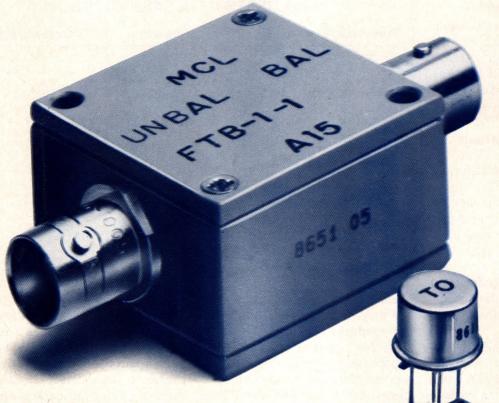
PC-board ATE market
to reach $1.1B by '93

Market Intelligence Research Company (Mountain View, CA) estimates that the world market for automatic test equipment (ATE) available on printed-circuit boards and subassemblies will reach $1.1 billion by 1993. MIRC expects that the fastest growing area of the market over the next few years will be the segment that makes and sells defect analyzers for manufactured goods. This segment should grow at a compound annual growth rate of 24%. Although functional-testing

products has recently lost market share, the market researchers predict that there will be renewed interest in those functional-testing products in the near future.

MIRC characterizes the pc-board ATE market as highly competitive. It discerns a trend toward combining and generally upgrading the types of boards currently available. These types include bareboard, in-circuit, and performance boards, as well as functional devices and defect analyzers for manufacturers' goods.

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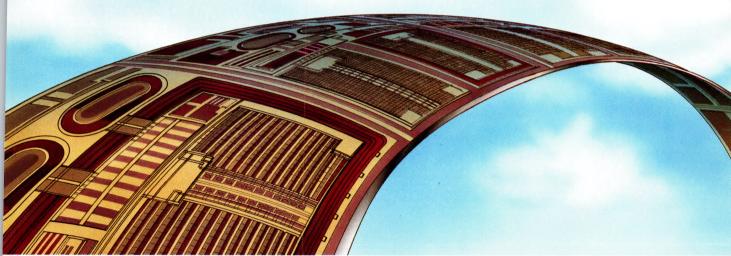
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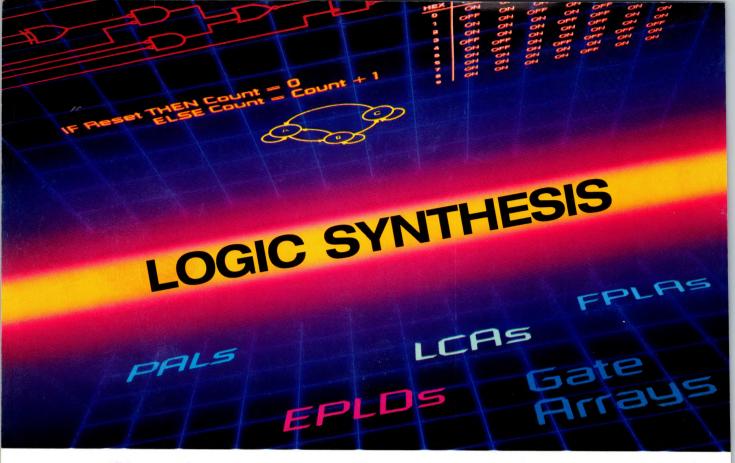
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